4.8V to 60V Input, 5A, Synchronous Step Down Converter

1 Features

- Wide input voltage range of 4.8V to 60V
- Junction temperature range: –40°C to +150°C
- Fixed 3ms internal soft start timer
- Peak current limit protection
- Thermal shutdown protection
- 0.8V 1% Internal Voltage Reference
- Fixed 160KHz Switching Frequency
- 80mΩ High-Side MOSFET
- Integrated low side n-channel MOSFET drivers
- High Efficiency at Light Loads with Pulse Skipping mode
- Low Dropout at Light Loads with Integrated BOOT Recharge FET
- 68V Input over voltage protection
- Operate at high duty cycles approaching 97%
- ESOP8 package

2 Applications

- Appliances, power and garden tools
- High-cell-count battery packs (E-Bike, E-Scooter)
- Motor drives, drones, Telecom
- Industrial Automation and Motor Control
- Vehicle Accessories: GPS, Entertainment
- USB Dedicated Charging Ports and Battery Chargers

3 Description

The PL880551 is a 60V, 5A, Synchronous step down regulator with an integrated high side MOSFET and low side n-channel MOSFET drivers. The device survives load dump pulses up to 68V. Current mode control provides simple external compensation and flexible component selection. A low ripple pulse skip mode reduces the no load supply current.

Under voltage lockout is internally set at 4.8V . The output voltage start up ramp is internally controlled to provide a controlled start up and eliminate overshoot.

PL880551 has configurable line drop compensation, configurable charging current limit. CC/CV mode control provides a smooth transition between constant current charging and constant voltage charging stages.

Additional features of the PL880551 include ultra low IQ and high light load efficiency, innovative peak current protection, integrated VCC bias supply and bootstrap diode, precision enable and input UVLO, and thermal shutdown protection with automatic recovery.

4 Typical Application Schematic

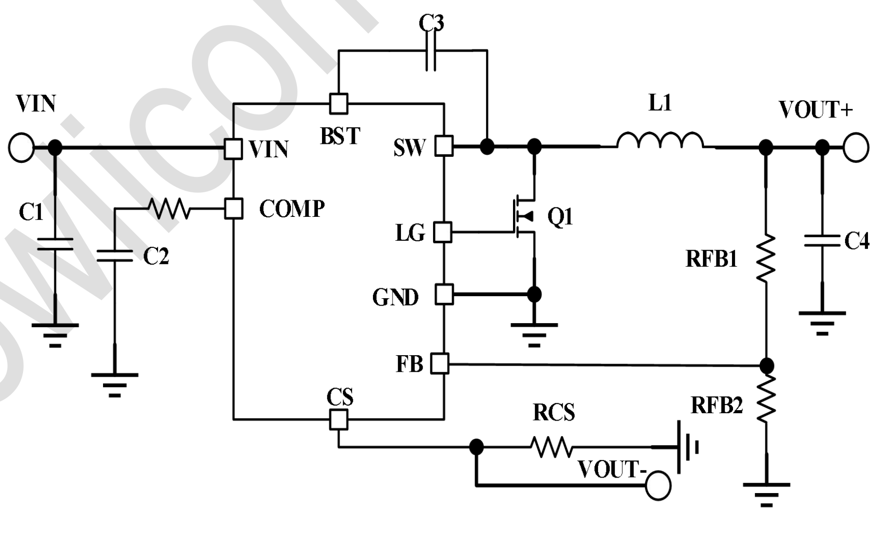


Fig. 4-1 Typical Application Schematic

5 Pin Configuration and Functions

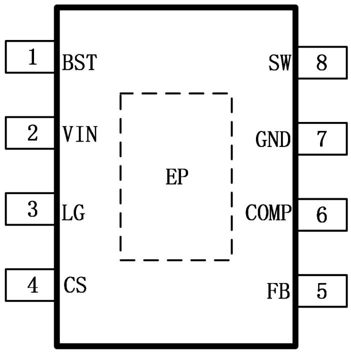


Fig. 5-1 Pin-Function

Pin		Description
Number	Name	
1	BST	Bootstrap gate drive supply.
2	VIN	Regulator supply input pin to high side power MOSFET and internal bias regulator. Connect directly to the input supply of the buck converter with short, low impedance paths.
3	LG	Output driver for low side MOSFET.
4	CS	Current sense input. Connect a 10mΩ to 100mΩ resistor between this pin and GND to program current limit.
5	FB	Feedback input of voltage regulation comparator.
6	COMP	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this terminal.
7	GND	Ground connection for internal circuits
8	SW	The source of the internal high-side power MOSFET and switching node of the converter.
9	EP	Exposed pad of the package. No internal electrical connection. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL880551	PL880551IES08A	ESOP8	4000	880551 RAAYMD

880551: Part Number
RAAYMD : RAA: LOT NO.; YMD: Package Date Code

7 Specifications

7.1 Absolute Maximum Ratings(Note1)

PARAMETER	MIN	MAX	Unit
VIN to GND	-0.3	70	V
LG to GND	-0.3	6.5	
FB to GND	-0.3	6.5	
CS to GND	-0.3	6.5	
BST to GND	-0.3	70	
BST to SW	-0.3	8	
SW to GND	-1.5	70	
COMP to GND	-0.3	6.5	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature	-40	+150	°C
V_{ESD}	HBM Human body model	2		kV

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	VIN	5.0	60	V
Temperature	Operating junction temperature range, T_J	-40	+150	°C

7.4 Thermal Information(Note 3)

Symbol	Description	ESOP8	Unit
θ_{JA}	Junction to ambient thermal resistance	41.1	°C/W
θ_{JC}	Junction to case thermal resistance	37.3	
θ_{JB}	Junction to board thermal resistance	30.6	

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1” square of 1 oz copper.

7.5 Electrical Characteristics

Typical values correspond to TJ = 25°C. Minimum and maximum limits apply over the full –40°C to 150°C junction temperature range unless otherwise indicated. VIN = 24V,unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN TERMINAL)						
VIN	Operating input voltage		4.8		60	V
VIN_{UV}	Internal under voltage lockout threshold			4.4		V
I_Q	Operating: non switching supply current	FB = 0.9V, TA = 25°C		1000		uA
VOLTAGE REFERENCE						
VFB	Voltage reference			0.8		V
LOW-SIDE DRIVERS						
ILDRV	Peak Source Current			0.37		A
	Peak Sink Current			1.15		A
Tr(LDRV)		CLOAD = 1000pF		40		ns
Tf(LDRV)		CLOAD = 1000pF		20		ns
HIGH-SIDE MOSFET						
Rds_on	On-resistance	VIN = 12V, BST-SW = 6V		80		mΩ
ERROR AMPLIFIER						
EA_Iin	Input current			50		nA
GAN	Error amplifier dc gain	VFB = 0.8 V		10,000		V/V
GW	Min unity gain bandwidth			2500		kHz
EA_source/sink	Error amplifier source/sink	V(COMP) = 1V, 100mV overdrive		±30		μA
CURRENT LIMIT						
V-CS	Current limit threshold			55		mV
THERMAL SHUTDOWN						
Thsd	Thermal shutdown			165		°C
Thsdhys	Thermal shutdown hysteresis			40		°C

Note:

Guaranteed by design, not tested in production.

8 Typical Characteristics

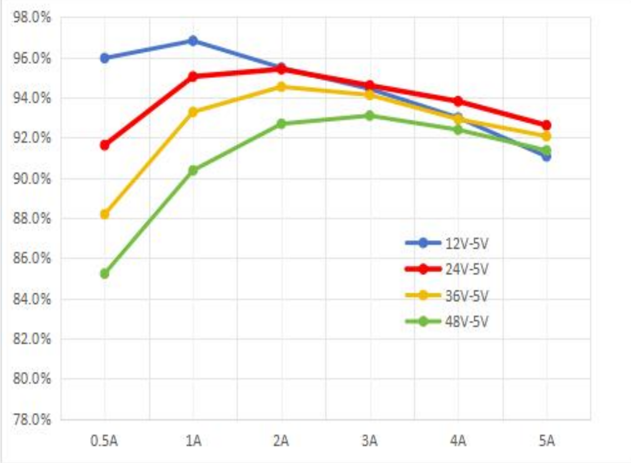
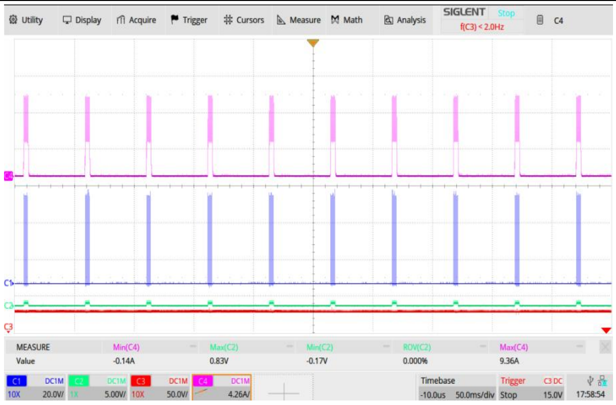


Fig.8-1 Efficiency



Ch1：SW Ch2：Vout Ch3：Vin Ch4：IL

Vin=48V Vout=5V

Fig.8-2 Short Circuit waveform

Ch1：SW Ch2：Vout Ch3：Vin Ch4：IL

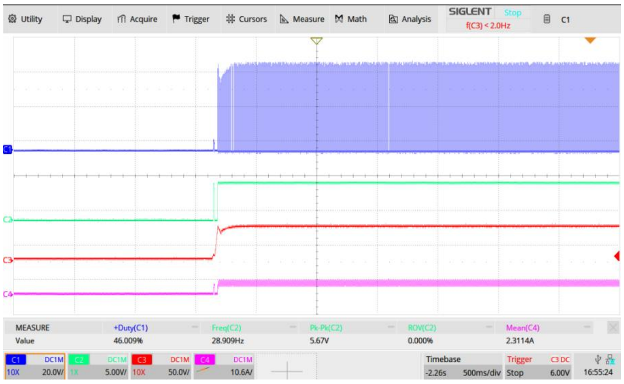
Vin=48V Vout=5V

Fig.8-3 Vin Start up waveform, Iout =0.1A

Ch1：SW Ch2：Vout Ch3：Vin Ch4：IL

Vin=48V Vout=5V

Fig.8-4 Vin Shut down waveform, Iout =0.1A



Ch1：SW Ch2：Vout Ch3：Vin Ch4：IL

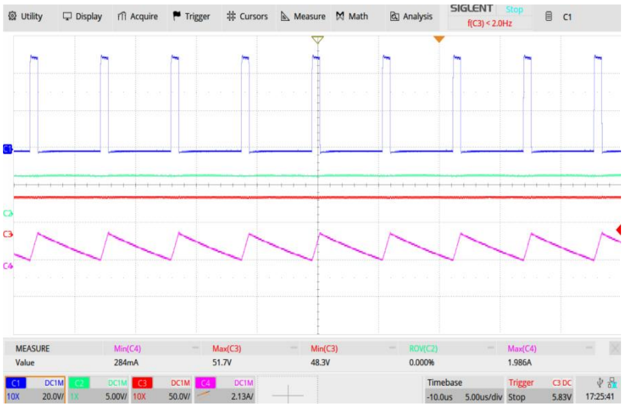
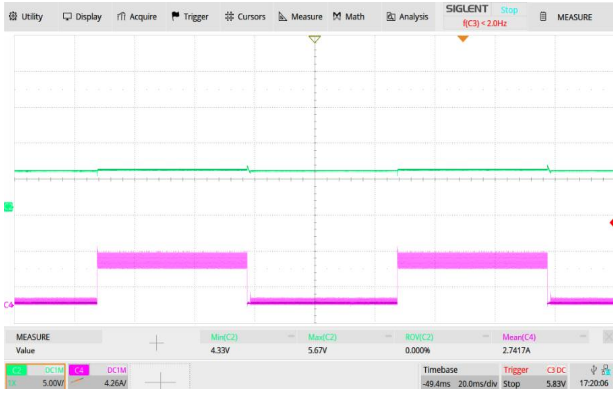
Vin=48V Vout=5V

Fig.8-5 Vin Start up waveform, Iout =3A

Ch1：SW Ch2：Vout Ch3：Vin Ch4：IL

Vin=48V Vout=5V

Fig.8-6 Vin Shut down waveform, Iout =3A

 Ch1：SW　Ch2：Vout　Ch3：Vin　Ch4：IL Vin=48V Vout=5V Fig.8-7　Steady State waveform, Iout =5A	 Ch2：Vout　Ch4：Iout Vin=48V Vout=12V Fig.8-8　Dynamic Load waveform, Iout =0.1-5A

9 Detailed Descriptions

9.1 Overview

The PL880551 is a 60V, 5A, Synchronous step-down (buck) regulator with an integrated high side n-channel MOSFET and low side n-channel MOSFET drivers. The device implements constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation.

PL880551 has configurable line drop compensation, configurable charging current limit. CC/CV mode control provides a smooth transition between constant current charging and constant voltage charging stages.

The integrated 80mΩ high side MOSFET supports high efficiency power supply designs capable of delivering 5 amperes of continuous current to a load. The gate drive bias voltage for the integrated high side MOSFET is supplied by a bootstrap capacitor connected from the BST to SW terminals. An automatic BST capacitor recharge circuit allows the PL880551 to operate at high duty cycles approaching 97%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application.

Output over voltage transients are minimized by an Over voltage Transient Protection (OVP) comparator. When the OVP comparator is activated, the high side MOSFET is turned off and remains off until the output voltage is less than 108% of the desired output voltage.

The PL880551 includes an internal soft-start circuit that slows the output rise time during start-up to reduce in- rush current and output voltage overshoot. Output overload conditions reset the soft-start timer. When the overload condition is removed, the soft-start circuit controls the recovery from the fault output level to the nominal regulation voltage. A frequency foldback circuit reduces the switching frequency during start-up and over current fault conditions to help maintain control of the inductor current.

9.2 Functional Block Diagram

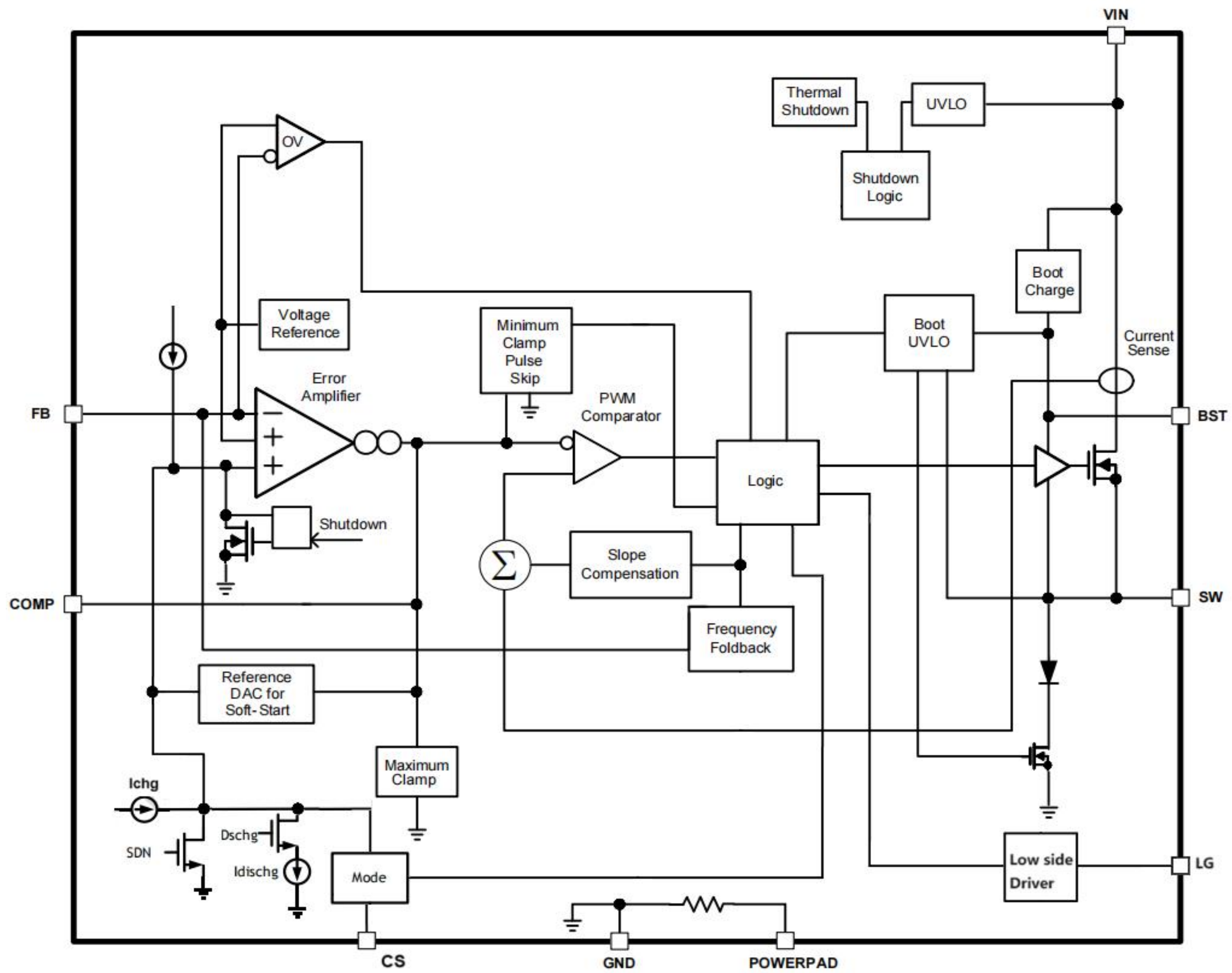


Fig. 9-2 Block Diagram

9.3 Fixed Frequency PWM Control

The PL880551 uses fixed frequency, peak current mode control with adjustable switching frequency. The output voltage is compared through external resistors connected to the FB terminal to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output at the COMP terminal controls the high side power switch current. When the high side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch is turned off. The COMP terminal voltage will increase and decrease as the output current increases and decreases. The device implements current limiting by clamping the COMP terminal voltage to a maximum level. The pulse skipping Eco-mode is implemented with a minimum voltage clamp on the COMP terminal.

9.4 Slope Compensation Output Current

The PL880551 adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

9.5 Pulse Skip mode

The PL880551 operates in a pulse skipping mode at light load currents to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse skipping current threshold, the device enters pulse skipping mode. The pulse skipping current threshold is the peak switch current level corresponding to a nominal COMP voltage of 600mV. When in this mode, the COMP terminal voltage is clamped at 600mV and the high side MOSFET is inhibited. Since the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the COMP terminal voltage. The high side MOSFET is enabled and switching resumes when the error amplifier lifts COMP above the pulse skipping threshold. The output voltage recovers to the regulated value,and COMP eventually falls below the mode pulse skipping threshold at which time the device again enters pulse skipping mode. The internal PLL remains operational when in pulse skipping mode. When operating at light load currents in pulse skipping mode, the switching transitions occur synchronously with the external clock signal.

9.6 Low Dropout Operation and Bootstrap Voltage (BST)

The PL880551 provides an integrated BST strap voltage regulator. A small capacitor between the BST and SW terminals provides the gate drive voltage for the high side MOSFET. The BST capacitor is refreshed when the high side MOSFET is off and the external low side MOSEFT conducts. The recommended value of the BST capacitor is 0.1μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended for stable performance over temperature and voltage.

Since the gate drive current sourced from the BST capacitor is small, the high side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 100%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance and the printed circuit board resistance.

9.7 Error Amplifier

The PL880551 voltage regulation loop is controlled by a transconductance error amplifier. The error amplifier compares the FB terminal voltage to the lower of the internal soft-start voltage or the internal 0.8V voltage reference. The transconductance (gm) of the error amplifier is 350μA/V during normal operation. During soft- start operation, the transconductance is reduced to 78μA/V and the error amplifier is referenced to the internal soft-start voltage.

The frequency compensation components (capacitor, series resistor and capacitor) are connected between the error amplifier output COMP terminal and GND terminal.

9.8 Low side driver(LG)

The PL880551provides low-side drivers at the LG pin. driver is capable of sourcing 0.37 A and sinking 1.15 A peak current.

9.9 Internal Soft Start

The PL880551 employs an internal soft start control ramp that allows the output voltage to gradually reach a steady state operating point, thereby reducing start up stresses and current surges. The soft start feature produces a controlled, monotonic output voltage start up. The soft start time is internally set to 3ms.

9.10 Regulation Comparator

The feedback voltage at FB is compared to an internal 0.8V reference. The PL880551 voltage regulation loop regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage, V_{REF}. A resistor divider programs the ratio from output voltage V_{OUT} to FB. For a target V_{OUT} set point, calculate R_{FB2} based on the selected R_{FB1} using

Equation 1:

$$R_{FB2} = \frac{0.8V}{V_{OUT}-0.8V} \times R_{FB1} \quad (1)$$

9.11 Line drop compensation

When USB charging cable line is long and resistance is high, there will be some significant voltage drop on the cable. Portable device will see much lower input voltage. If the voltage across the load input terminals is too low, it will affect the charge time for the load. It is recommended to adjust the output voltage of charger to compensate this voltage drop. PL880551 has an configurable line drop compensation feature. The line drop compensation value can be programmed by the top feedback resistor RFB1 in Fig 4.1. The line compensation voltage can be roughly calculated using **Equation 2:**

$$\Delta Vout = \frac{Rcs(m\Omega) * Iout(A) * 15 * RFB1(k\Omega)}{200k\Omega} \quad (2)$$

Rcs is the sum of current sensing resistor on CS pin, all of the parasitic resistance on PCB board and GND pin. Iout is output load current going through Rcs. RFB1 is the top feedback resistor.

9.12 CC/CV control mode and average load current limiting

PL880551 has a CC/CV control mode. The load current is sensed . When average load current is high enough, constant-current loop will be dominant and limit the average load current to a value configured by resistor on CS pin. The Relationship using **Equation 3:**

$$R_{CS(m\Omega)} = \frac{55(mV)}{I_{load}(A)} \quad (3)$$

9.13 Over voltage Protection

The PL880551 incorporates an output over voltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB terminal voltage is lower than the internal reference voltage for a considerable time,the output of the error amplifier will increase to a maximum voltage corresponding to the peak current limit threshold. When the overload condition is removed, the regulator output rises and the error amplifier output transitions to the normal operating level. In some applications, the power supply output voltage can increase faster than the response of the error amplifier output resulting in an output overshoot.

The OVP feature minimizes output overshoot when using a low value output capacitor by comparing the FB terminal voltage to the rising OVP threshold which is nominally 109% of the internal voltage reference. If the FB terminal voltage is greater than the rising OVP threshold, the high side MOSFET is immediately disabled to minimize output overshoot. When the FB voltage drops below the falling OVP threshold which is nominally 106% of the internal voltage reference, the high side MOSFET resumes normal operation.

9.14 Thermal Shutdown

The PL880551 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 175°C. The high side MOSFET stops switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature falls below 164°C, the device reinitiates the power up sequence controlled by the internal soft-start circuitry.

10 Applications and Implementation

10.1 Selecting the Inductor

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current.

For a given ripple, the inductance terms in continuous mode are as ***Equation 4.***

$$L=\frac{V_{OUT}}{f_s\times\Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

where: f_s is operating frequency, kHz

ΔI_L is maximum inductor ripple current, A, usually select 20~40% maximum output current.

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

10.2 Output Capacitor (C_{OUT})

Select a ceramic output capacitor to limit the capacitive voltage ripple at the converter output. This is the sinusoidal ripple voltage that is generated from the triangular inductor current ripple flowing into and out of the capacitor. Select an output capacitance using ***Equation 5*** to limit the voltage ripple component to 0.5% of the output voltage.

$$C_{OUT} \geq \frac{\Delta I_L}{8\times F_{SW}\times V_{OUT(ripple)}} \quad (5)$$

Substituting $\Delta I_{L(nom)}$ of 447mA gives C_{OUT} greater than 3.1μF. With voltage coefficients of ceramic capacitors taken in consideration, a 22μF, 25V rated capacitor with X7R dielectric is selected.

10.3 Input Capacitor (C_{IN})

An input capacitor is necessary to limit the input ripple voltage while providing AC current to the buck power stage at every switching cycle. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the VIN and GND pins of the PL880551. The input capacitors conduct a square wave current of peak to peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR related ripple component, the peak-to-peak ripple voltage amplitude is given by ***Equation 6***.

$$V_{IN(ripple)} = \frac{I_{OUT}\times D\times(1-D)}{F_{SW}\times C_{IN}} + I_{OUT}\times R_{ESR} \quad (6)$$

The input capacitance required for a load current, based on an input voltage ripple specification (ΔVIN), is given by ***Equation 7***:

$$C_{IN} \geq \frac{I_{OUT}\times D\times(1-D)}{F_{SW}\times(V_{IN(ripple)}-I_{OUT}\times R_{ESR})} \quad (7)$$

The recommended high-frequency input capacitance is 2.2μF or higher. Ensure the input capacitor is a high quality X7S or X7R ceramic capacitor with sufficient voltage rating for C_{IN}. Based on the voltage coefficient of ceramic capacitors, choose a voltage rating of twice the maximum input voltage. Additionally, some bulk capacitance is required if the PL880551 is not located within approximately 5cm from the input voltage source. This capacitor provides parallel damping to the resonance associated with parasitic inductance of the supply lines and high Q ceramics.

11 PCB Layout

11.1 Guideline

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Place the input decoupling capacitor, Low side MOSEFT, and the PL880551 (VIN, SW, and GND) as close to each other as possible.
2. Keep the power traces very short and fairly wide, especially for the SW node. This can help greatly reduce voltage spikes on the LG & SW node and lower the EMI noise level.
3. Run the feedback trace as far from the inductor and noisy power traces (like the SW node) as possible.
4. Place thermal vias with 15mil barrel diameter and 40mil pitch (distance between the centers) under the exposed pad to improve thermal conduction.

11.2 Application Examples

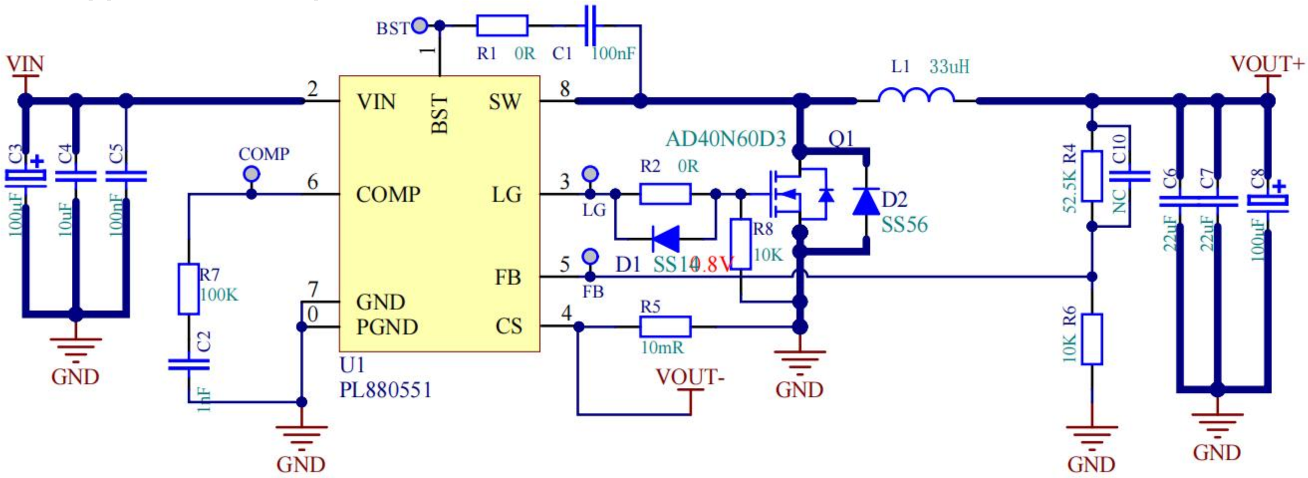


Fig. 11-2-1 Schematic

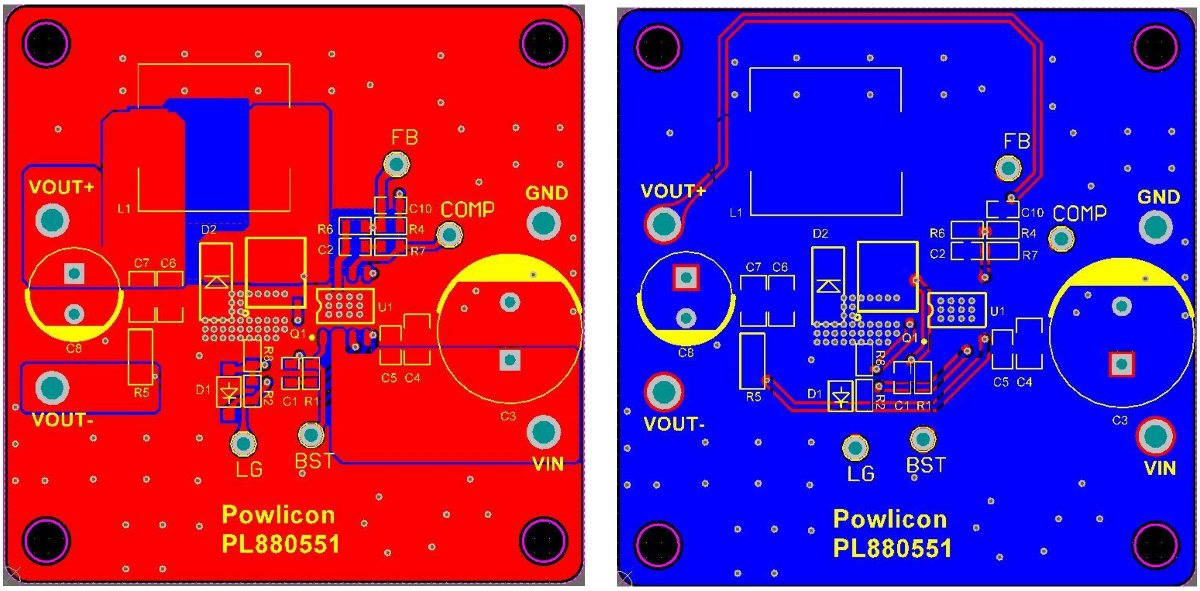
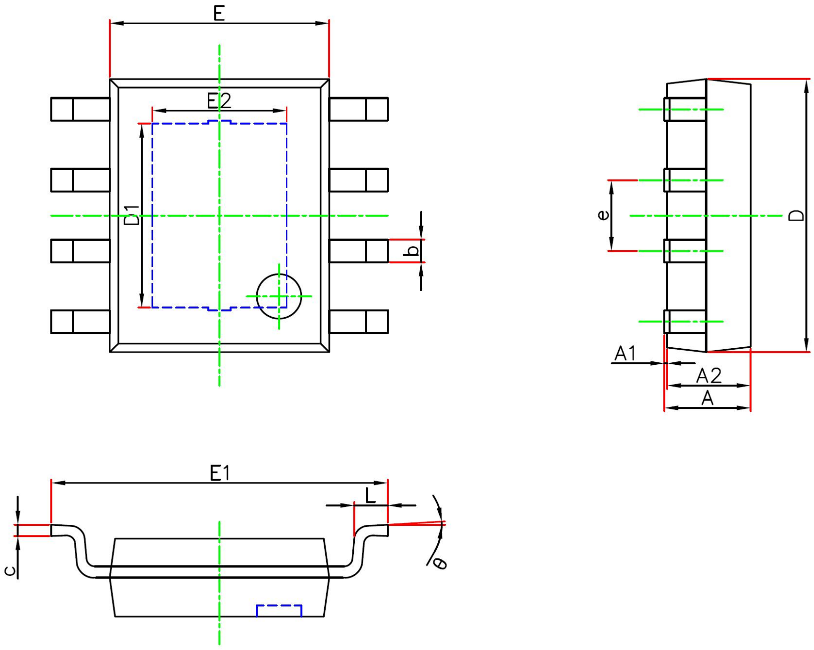


Fig. 11-2-3 PCB

12 Packaging Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°