55V, 600mA Monolithic Step-Down Switching Regulator

1 Features

- 600mA continuous output current capability
- 4.5V to 55V wide operating input range
- Integrated 80V, 550mΩ high side and 80V, 350mΩ low side power MOSFET switches
- Up to 95% efficiency
- Internal Soft-Start limits the inrush current at turn-on
- Internal compensation to save external components
- Input Under-Voltage Lockout
- Input over-voltage protection to protect device from working in high voltage and high current condition
- Output Over-Voltage Protection
- Output short protection
- Over-Temperature Protection
- Pulse skip mode at light load to improve light load efficiency
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 600k Switching Frequency
- Fewest external components and intensive internal protection features
- SOT23-6L Package

2 Applications

- Power Meters
- Distributed Power Systems
- Battery Chargers
- Pre-Regulator for Linear Regulators
- WLED Drivers

3 Description

PL88103 is a monolithic 55V, 600mA step-down switching regulator. PL88103 integrates a 80V 550mΩ high side and a 80V, 350mΩ low side MOSFETs to provide 600mA continuous load current over a 4.5V to 55V wide operating input voltage. Peak current mode control provides fast transient responses and cycle-by-cycle current limiting.

4 Typical Application Schematic

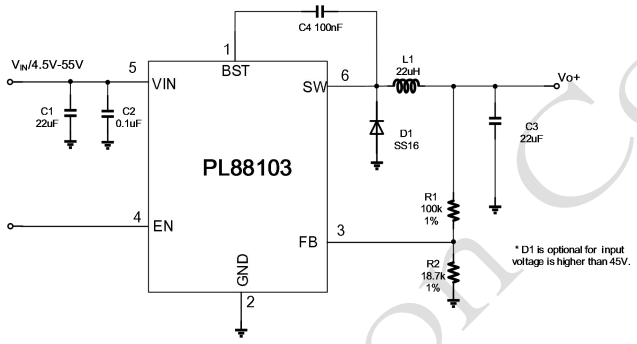


Fig. 1 Schematic

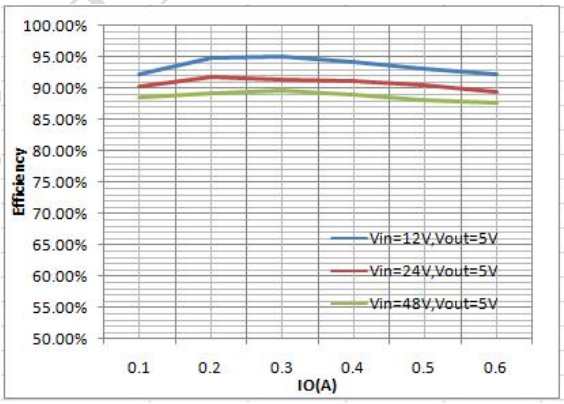


Fig. 2 Efficiency

5 Pin Configuration and Functions

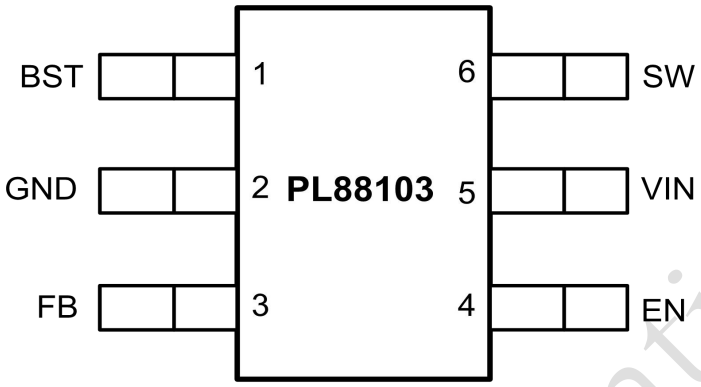


Fig.3 SOT23-6L Package

PL88103 Pin-Functions

Pin		Description
Number	Name	
1	BST	Boot-Strap pin Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver.
2	GND	Ground.
3	FB	Feedback Input. FB senses the output voltage. Connect FB with a resistor divider connected between the output and ground. FB is a sensitive node. Keep FB away from SW and BST pin.
4	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. EN pin is pulled to VIN internally by a larger resistor.
5	VIN	Power Input. Vin supplies the power to the IC. Supply Vin with a 4.5V to 55V power source. Bypass Vin to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors close to Vin and GND pins.
6	SW	Power Switching pin. Connect this pin to the switching node of inductor.

6 Device Marking Information

Order Information	Label Part NO.	Package	Package Qty	Top Marking
PL88103	**PL88103ISO06A**	**SOT23-6L**	**3000**	**D3YMD**

PL88103: Part Number
D3YMD: D3: Part Number YMD:Package Date Code

7 Specifications

7.1 Absolute Maximum Ratings (Note1)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	-0.3	65	V
	V_{EN} to GND	-0.3	6	
	V_{FB} to GND	-0.3	6	
	V_{BST} to V_{SW}	-0.3	6	
	V_{SW} to GND	-1	V_{IN}+ 0.3	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	TYP	MAX	UNIT
T_{ST}	Storage Temperature Range	-65		150	°C
T_J	Junction Temperature			+160	°C
T_L	Lead Temperature			+260	°C
V_{ESD}	HBM Human body model		2		kV

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	6.5	55	V
	FB	-0.3	3.3	V
Output Voltages	V_{OUT}	0.5	V_{IN}*D_{max}	V
Output Current	I_{OUT}	0	600	mA
Temperature	Operating junction temperature range, T_J	-40	+125	°C

7.4 Thermal Information(Note 3)

Symbol	Description	SOT23-6L	Unit
θ_{JA}	Junction to ambient thermal resistance	180	°C/W
θ_{JC}	Junction to case thermal resistance	34	

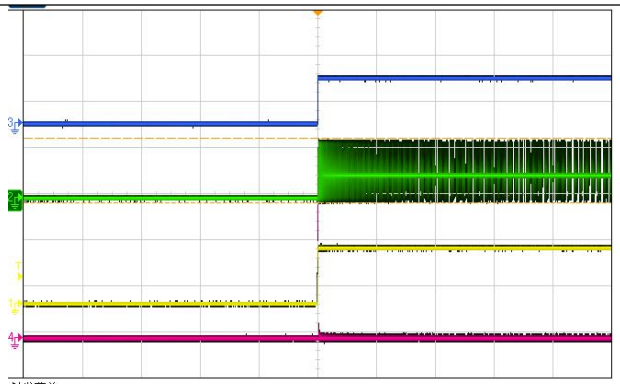
Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

7.5 Electrical Characteristics(Typical at Vin = 12V, T_J=25°C, unless otherwise noted.)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
MOSFET						
I_{leak_sw}	High-Side Switch Leakage Current	V_{EN} = 0V, V_{SW}= 0V		0	10	μA
$R_{DS(ON)\_H}$	High-Side Switch On-Resistance	I_{OUT} = 600mA, V_{OUT} = 3.3V		550		mΩ
$R_{DS(ON)\_L}$	Low-Side Switch On-Resistance	I_{OUT} = 600mA, V_{OUT} = 3.3V		350		mΩ
SUPPLY VOLTAGE (VIN)						
V_{UVLO_up}	Minimum input voltage for startup			4.6		V
V_{UVLO_down}				4.3		V
V_{UVLO_hys}				0.4		
$I_{Q\text{-}NONSW}$	Operating quiescent current	V_{FB} =0.8V		250		μA
CONTROL LOOP						
F_{oscb}	Buck oscillator frequency			600		kHz
V_{FB}	Feedback Voltage	6.5V ≤ VIN ≤ 33V		0.8		V
V_{FB_OVP}	Feedback Over-voltage Threshold			1.1* V_{FB}		V
D_{max}	Maximum Duty Cycle(Note 4)			95		%
T_{on}	Minimum On Time(Note 4)			100		ns
PROTECTION						
V_{inovp}	Input Over voltage protection			62		V
Th_{sd}	Thermal Shutdown(Note 4)			150		°C
Th_{sdhys}	Thermal Shutdown Hysteresis(Note 4)			40		°C

Note:
4) Guaranteed by design, not tested in production.

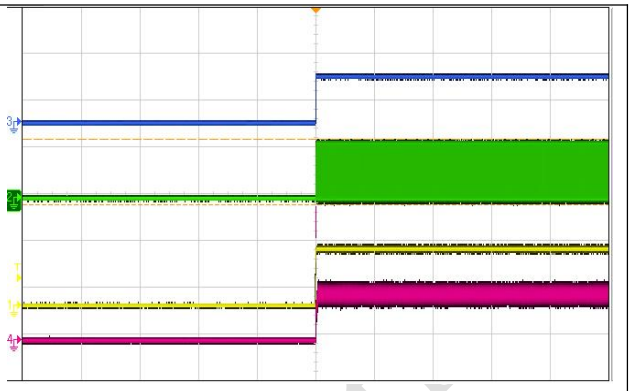
8 Typical Characteristics



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=5V

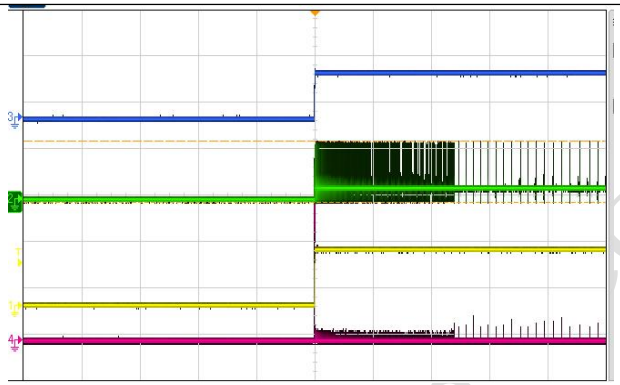
Fig.4 Start up waveform, Iout =0A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=5V

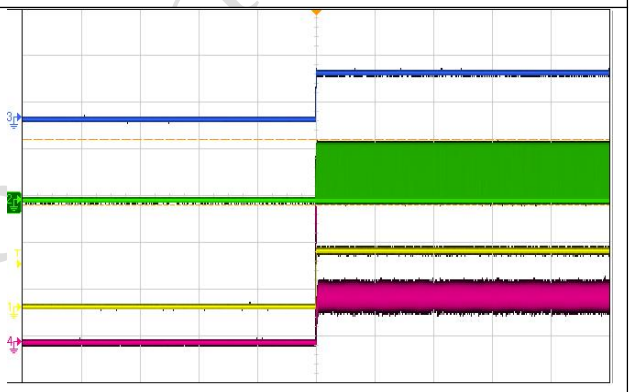
Fig.5 Start up waveform, Iout =0.6A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=5V

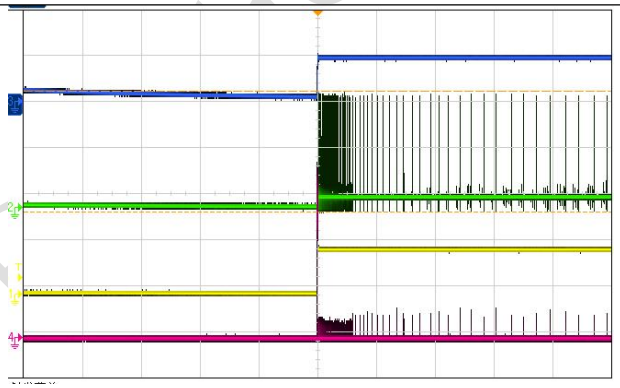
Fig.6 Start up waveform, Iout =0A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=5V

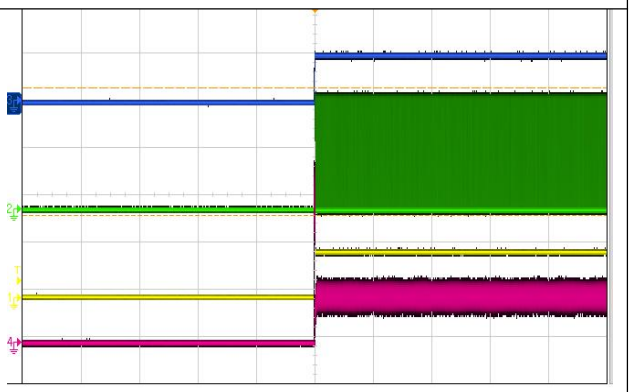
Fig.7 Start up waveform, Iout =0.6A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=48V Vout=5V

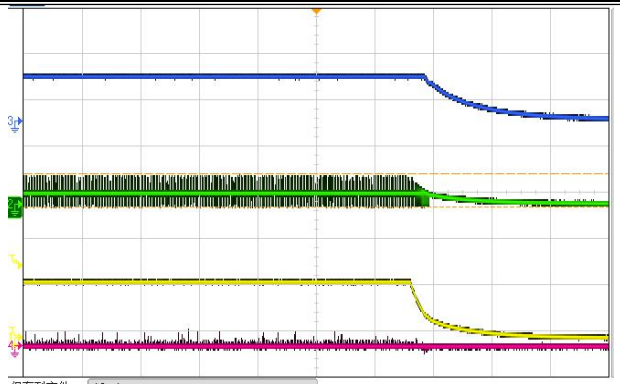
Fig.8 Start up waveform, Iout =0A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=48V Vout=5V

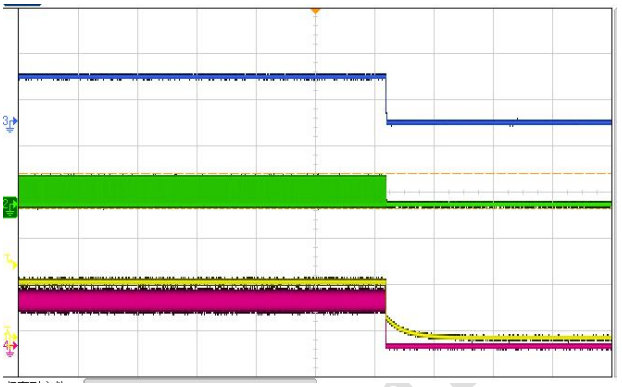
Fig.9 Start up waveform, Iout =0.6A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=5V

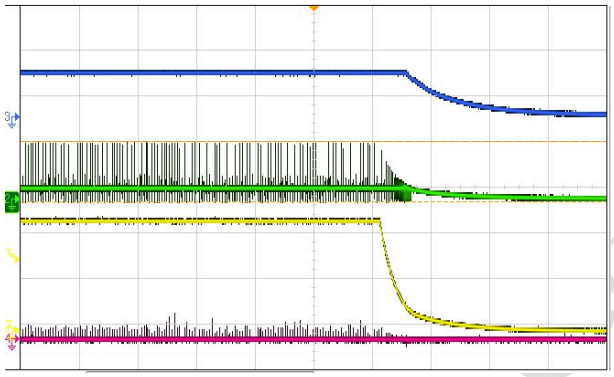
Fig.10 Shut down waveform, Iout =0A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=5V

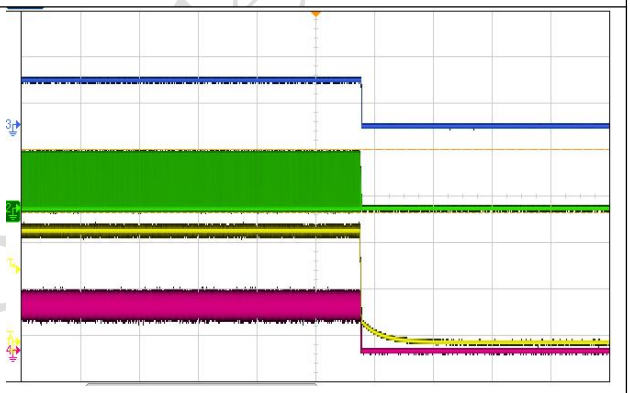
Fig.11 Shut down waveform, Iout =0.6A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=5V

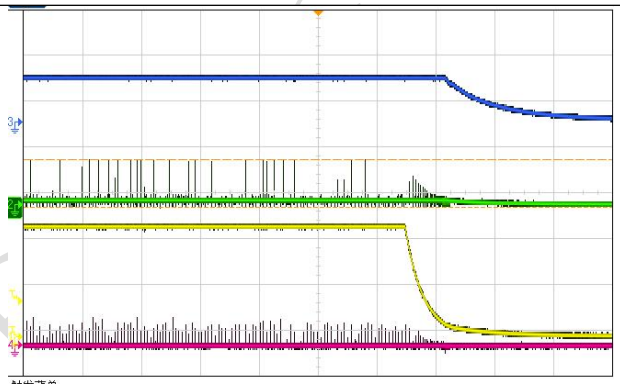
Fig.12 Shut down waveform, Iout =0A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=5V

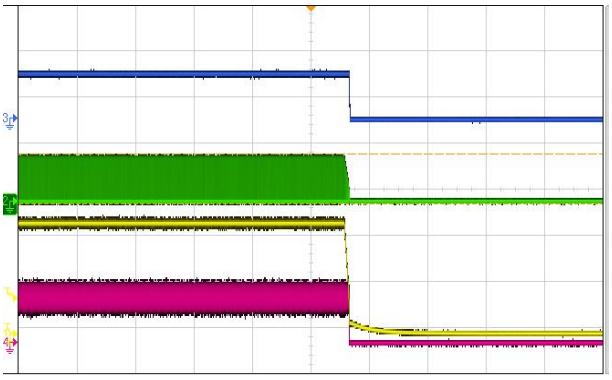
Fig.13 Shut down waveform, Iout =0.6A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=48V Vout=5V

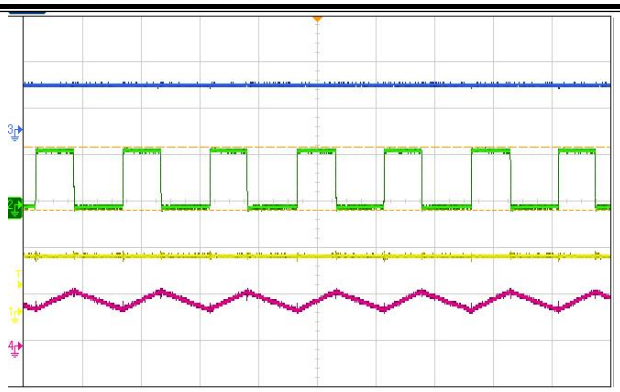
Fig.14 Shut down waveform, Iout =0A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=48V Vout=5V

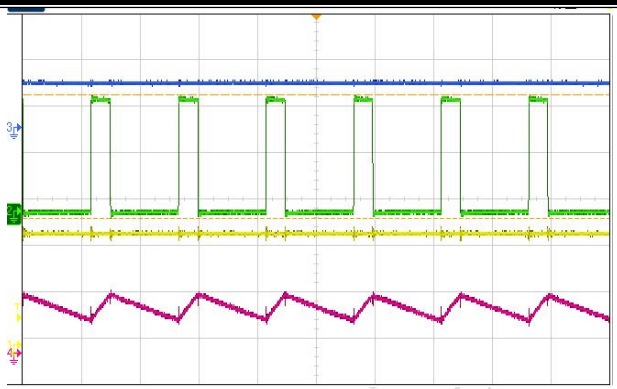
Fig.15 Shut down waveform, Iout =0.6A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=5V

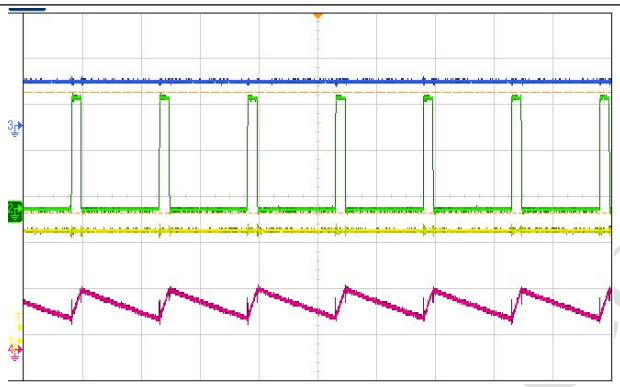
Fig.16 Steady State, Iout =0.6A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=5V

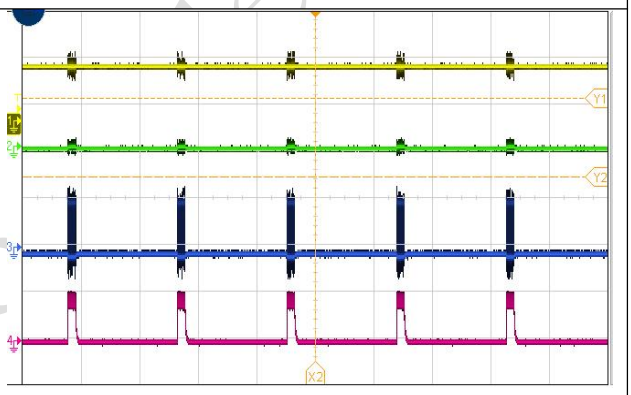
Fig.17 Steady State, Iout =0.6A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=48V Vout=5V

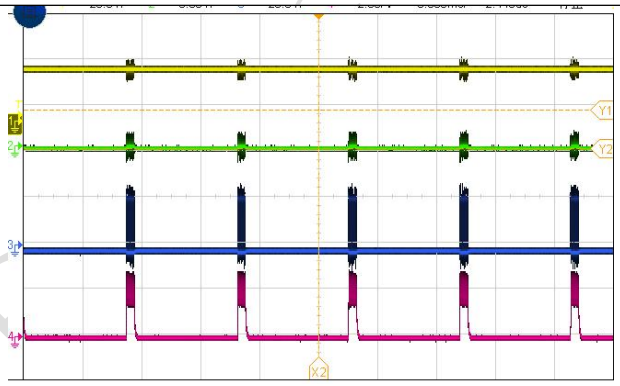
Fig.18 Steady State, Iout =0.6A



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=5V

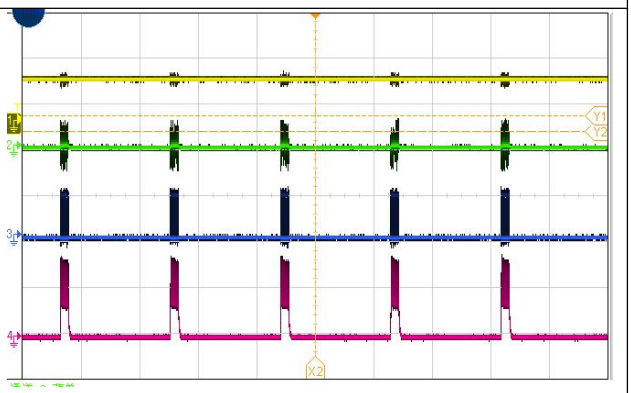
Fig.18 Short Circuit waveform



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=5V

Fig.20 Short Circuit waveform



CH1:VIN CH2:SW2 CH3:Vout CH4:IL

Vin=48V Vout=5V

Fig.21 Short Circuit waveform

9 Detailed Description

9.1 Overview

PL88103 is an easy to use synchronous step-down DC-DC converter that operates from 4.5V to 55V supply voltage. It is capable of delivering up to 600mA continuous load current with high efficiency and thermal performance in a very small solution size. PL88103 also integrates input over voltage and output over voltage protection. This feature helps customers to design a safe DC-DC converter easily.

9.2 Functional Block Diagram

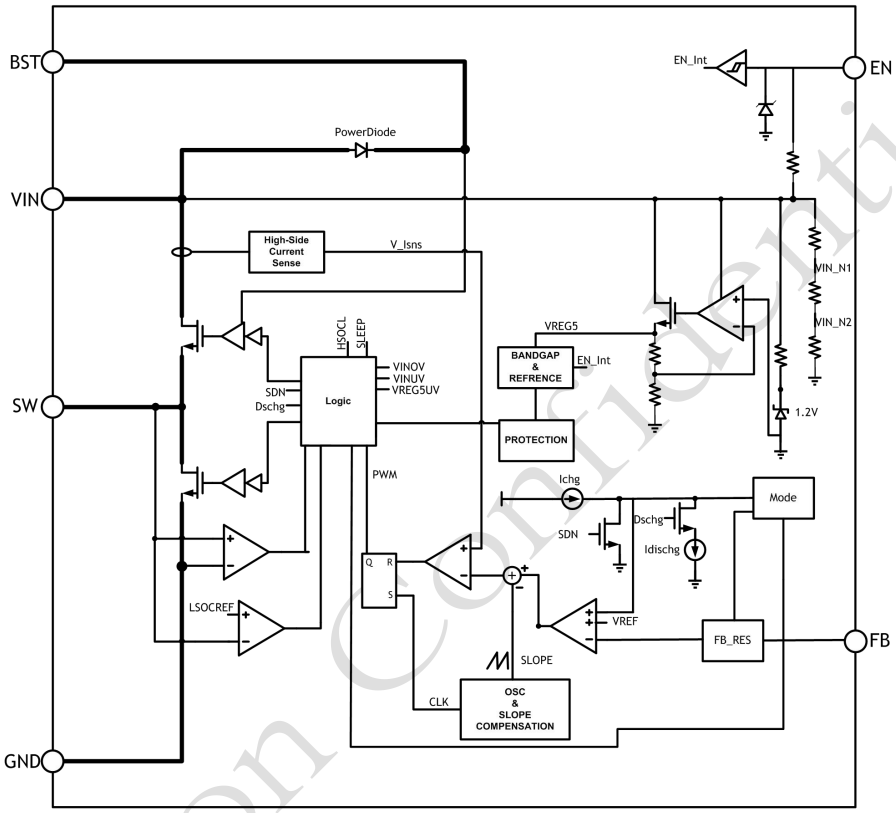


Fig.22 PL88103 Diagram

9.3 Peak Current Mode Control

PL88103 employs a fixed 600kHz frequency peak current mode control. The output voltage is sensed by an external feedback resistor string on FB pin and fed to an internal error amplifier. The output of error amplifier will compare with high side current sense signal by an internal PWM comparator. When the second signal is higher than the first one, the PWM comparator will generate a turn-off signal to turn off high side switch. The output voltage of error amplifier will increase or decrease proportionally with the output load current. PL88103 has a cycle-by-cycle peak current limit feature inside to help maintain load current in a safe region.

9.4 Sleep Operation for Light Load Efficiency

PL88103 has an internal feature to help improving light load efficiency. When output current is low, PL88103 will go into sleep mode.

9.5 Setting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. 1% resistance accuracy of this resistor divider is preferred. The output voltage value is set as equation 1 below (R_1 is the upper resistor, R_2 is the lower resistor).

$$V_{out}=V_{ref}\times\frac{R_1+R_2}{R_2} \quad (1)$$

V_{ref} is the internal reference voltage of PL88103, which is 0.8V.

9.6 Setting Enable Threshold

When the voltage at EN pin exceeds the threshold, PL88103 begins to work. When keeping EN low (below threshold), PL88103 stops working. The quiescent current of PL88103 is very low to maintain a good shut down operation for system. PL88103 has an internal pull up resistor to make sure IC work when EN pin is float. If an application requires to control EN pin, use open drain or open collector output logic circuit to interface with it.

When system needs a higher VIN UVLO threshold, the EN pin can be configured as shown in Figure 23 below.

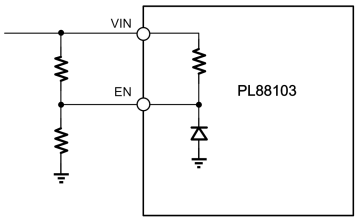


Fig.23 Adjustable VIN Under voltage Lockout

9.7 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 155°C typically. When the junction temperature drops below 110°C, IC will start to work again.

10 Application and Implementation

10.1 Inductor selection

An inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 25% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s\times\Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum peak current. The peak inductor current can be calculated by:

$$I_{L\_P}=I_{load}+\frac{V_{OUT}}{2\times f_s\times L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Where I_{load} is the load current.

The choice of inductor material mainly depends on the price vs. size requirements and EMI constraints.

10.2 Input capacitors selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C_{IN}) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2\times V_{OUT}$, where:

$$I_{CIN}=\frac{I_{load}}{2} \quad (5)$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN}=\frac{I_{load}}{f_s\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

C_{IN} is the input capacitance.

10.3 Output capacitors selection

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended.

Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_s\times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor and C_{OUT} is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the

capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulator. PL88103 is optimized for a wide range of capacitance and ESR values.

11 PCB Layout

11.1 Guideline

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R_1 and R_2, should be kept close to FB pin. V_{out} sensing path should stay away from noisy nodes, such as SW and BST signals. The ground of R2 should be connected directly to GND pin by a single point. An optional 47pF capacitor may be needed to improve the noise immunity for a poor placed PCB.
2. The input bypass capacitor C_2 must be placed as close as possible to V_{IN} pin and GND pin. Grounding for both the input and output capacitors should consist of localized top side planes. Make the GND plane as big as possible for best thermal performance.
3. Input capacitor, output capacitor, inductor and PL88103 should be placed evenly on the PCB board for the best thermal performance. Separate PL88103 from inductor as much as possible since they are the hottest components on the PCB.

11.2 Example

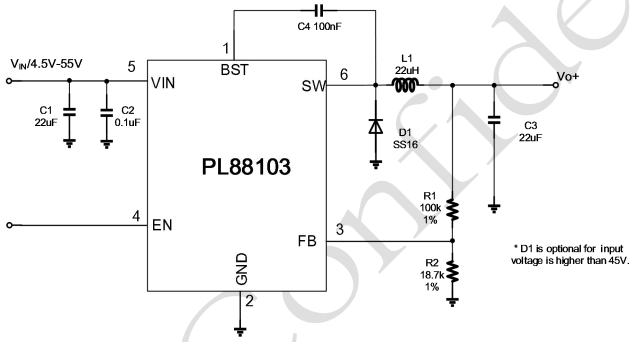


Fig 24 **Schematic**

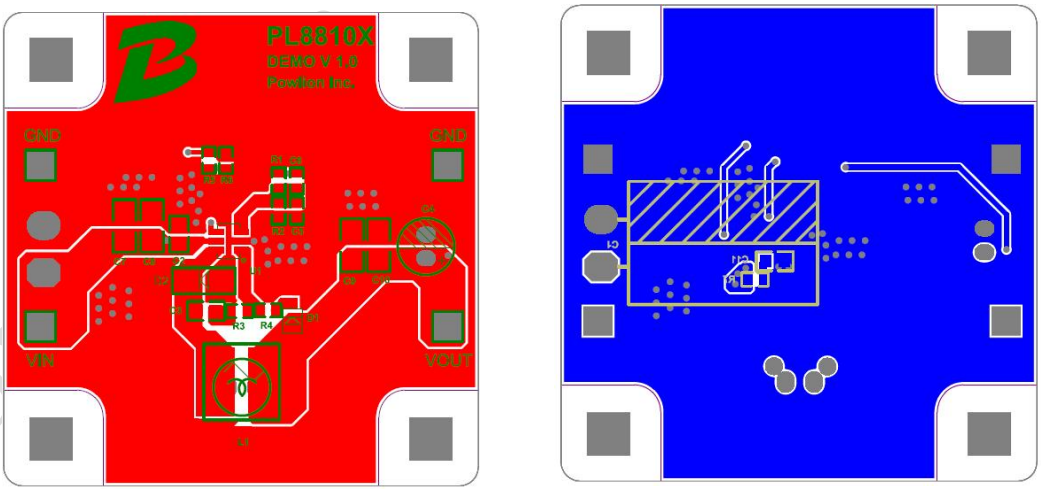
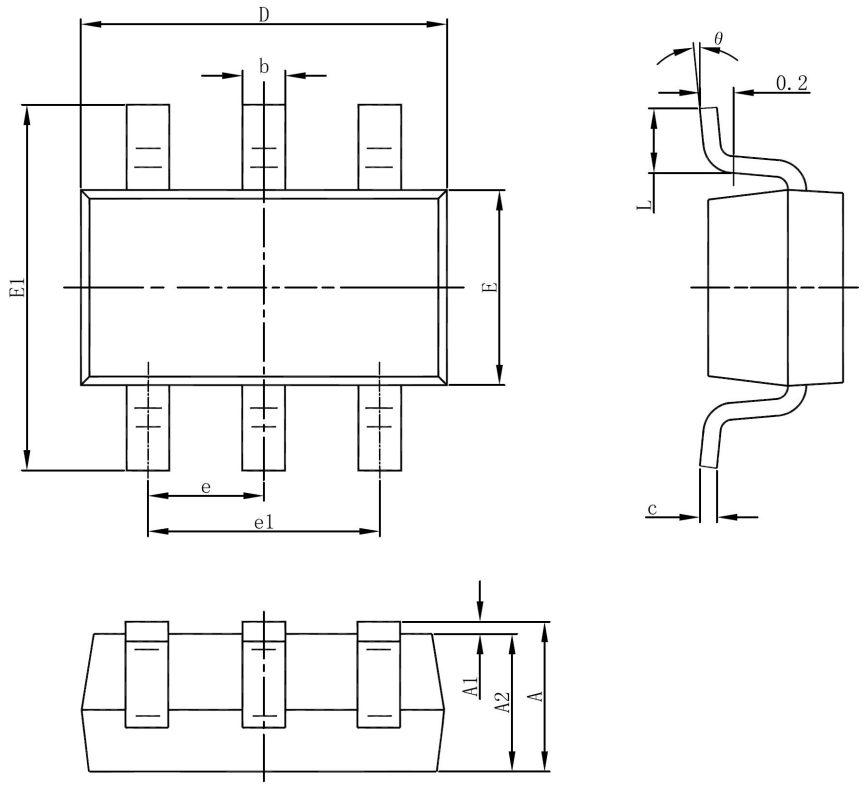


Fig 25 **PCB Layout**

12 Packaging Information

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

13 Version Control

版本	日期	撰写	页数	更新说明
Rev.1.0	2022-03-03	Victor	14	增加产品订购信息