24V,10A, Synchronous Boost Converter with Load Disconnect Control

1 Features

- Input Voltage Range :2.7V to 24V
- Output Voltage Range :4.5V to 24V
- Efficiency up to 91%: VIN = 3.3V, VBUS = 12, IOUT = 1.5A
- Two 18mΩ FETs Integrated
- Adjustable switching frequency up to 2.2MHz
- Programmable Cycle-by-Cycle Current Limit up to15A
- Hiccup Short Protection with Load Disconnect Drive
- DCM or USM Operation under light load
- Input Under-Voltage Lockout
- Output Over-Voltage Protection at fixed 25.2V
- Over-Temperature Protection
- QFNWB3.5*4.5-20L Package

2 Applications

- Portable POS terminal
- Bluetooth Speaker
- E-Cigarette
- Thunderbolt Interface
- USB Type-C Power Delivery

3 Description

The PL32001 is a 24V synchronous Boost converter with the gate driver built in for load disconnect. The PL32001 integrates two low on resistance power FETs: A 18mΩ switching FET and a 18mΩ rectifier FET.

The PL32001 uses the adaptive constant off time peak current mode control. PL32001 has an internal feature to help improving light load efficiency. When output current is low, PL32001 will go into DCM mode.

The PL32001 includes configurable features include programmable cycle-by-cycle current limit, programmable switching frequency functions and mode selection functions.

The PL32001 could isolate the output from input side when shutdown. Once the output is shorted, it enters into the hiccup mode to lower the thermal stress and can recover automatically after the short condition releases. Additionally, the PL32001 also has OVP and thermal protection to avoid the fault operation.

The PL32001 is in a 3.5-mm x 4.5-mm 20-pin QFNWB package with enhanced thermal dissipation.

4 Typical Application Schematic

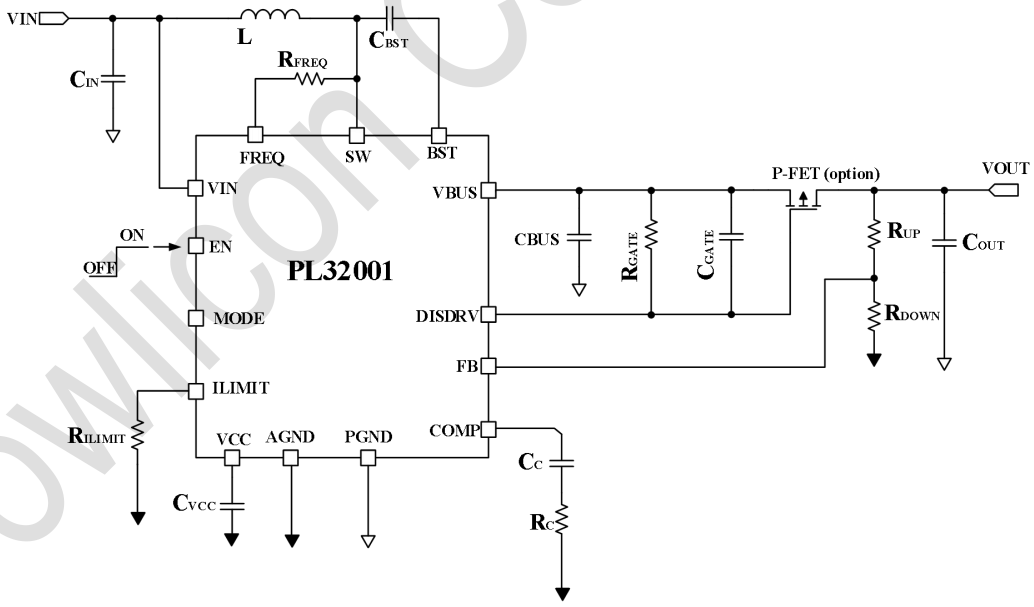


Fig. 4-1 Typical Application Schematic

5 Pin Configuration and Functions

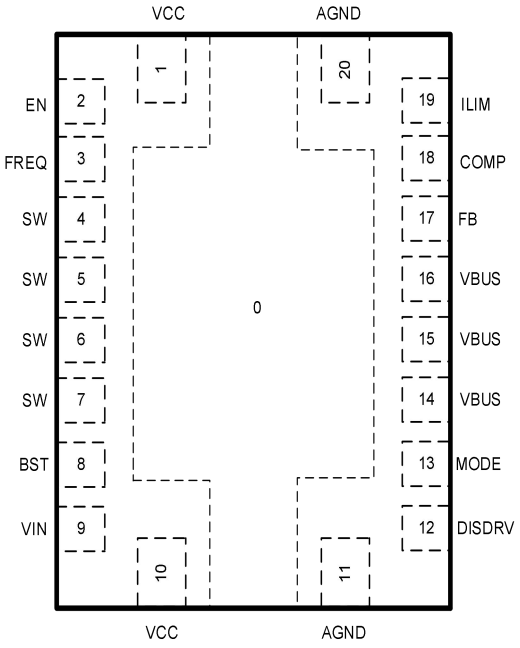


Fig. 5-1 Top view

Tab.5-1 PL32001 Pin-Functions

Pin		Description
Number	Name	
1,10	VCC	Output of internal regulator, A ceramic capacitor of more than 4.7μF is required between this pin and ground.
2	EN	Enable pin. Pull high to turn on the IC, don't float.
3	FREQ	The switching frequency is programmed by a resistor between this pin and the SW. This pin can't be float in application.
4,5,6,7	SW	Power switching pin of boost converter, common node of LSFET drain and HSFET source.Connect the coil to this pin and power input.
8	BST	Boot strap pin Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver.
9	VIN	Input supply pin. Bypass VIN to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors close to VIN and GND pins.
11,20	AGND	Analog ground.
12	DISDRV	A gate drive output for the external disconnect FET. Connect the DISDRV pin to the gate of the external FET. Leave it floating if not using the load disconnect function.
13	MODE	Operation mode selection. 2MΩ internal resistor connects this pin to VREF.Logic high enables CCM mode. Logic low enables DCM mode.Floating enables USM mode.
14,15,16	VBUS	Output pin of boost converter, connect to the drain of HSFET internally.
17	FB	Feedback Input. FB senses the output voltage, connect FB with a resistor divider connected between the output and ground. FB is a sensitive node, keep FB away from SW and BST pin.
18	COMP	Output of internal error amplifier, loop compensation network connect to COMP and AGND .COMP is a sensitive node, keep COMP away from SW and BST pin.
19	ILIM	Adjustable LSFET peak current limit. Connect a resistor to AGND.
0	PGND	Power ground. The source of LSFET connect to PGND internally.

6 Device Marking Information

Tab. 6-1 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL32001	PL32001IQN20A	QFN3.5X4.5-20L	4000	32001 RAAYMD

PL32001: Part Number
RAAYMD: RAA: LOT NO.; YMD: Package Date

7 Specifications

7.1 Absolute Maximum Ratings (Note1)

Over operating free-air temperature range (unless otherwise noted).

Tab. 7-1-1 Absolute Maximum Ratings

		MIN	MAX	Unit
Voltage range at terminals (Note2)	BST	-0.3	SW+6.5	V
	VIN, SW, DISDRV, VBUS, EN	-0.3	24	
	FB, COMP, ILIMIT, VCC, FREQ	-0.3	6.5	

7.2 Handling Ratings

Tab. 7-2-1 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+160	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model	2	4	kV
T_A	Operating Ambient Temperature Range	-40	85	°C

7.3 Recommended Operating Conditions (Note 3)

Tab. 7-3-1 Recommended Operating Conditions

		MIN	MAX	Unit
Voltage range at terminals(Note2)	VIN	2.7	24	V
	VBUS	4.5	24	
	BST	0	SW+5	
	EN	0	V_{IN}	
	SW,DISDRV,FREQ	0	V_{BUS}	
	FB,COMP,ILIMIT,VCC,MODE	0	5	

7.4 Thermal Information(Note 4)

Tab. 7-4-1 Thermal Information

Symbol	Description	QFN3.5X4.5-20L	Unit
θ_{JA}	Junction to ambient thermal resistance	30	°C/W
θ_{JC}	Junction to case thermal resistance	10	

Notes:
1) Exceeding these ratings may damage the device.
2) All voltage values are with respect to network ground terminal.
3) The device function is not guaranteed outside of the recommended operating conditions.
4) Measured on approximately 1" square of 1 oz copper.

7.5 Electrical Characteristics

(Typical at VBUS = 12V, VIN = 3.6V, T_J=25°C, unless otherwise noted.)

Tab. 7-5-1 Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply Section						
VIN	VIN operating range		2.7		24	V
V_{UV_VIN}	VIN UVLO threshold voltage	when VIN < V_{UV_VIN}, IC turn off, falling edge		2.43		V
$V_{UV\_VIN\_HYS}$	VIN UVLO hysteresis voltage	after VIN > V_{UV_VIN}+ $V_{UV\_VIN\_HYS}$, IC restore operation		0.27		V
VCC	VCC regulation voltage	I_{VCC}=2mA, VIN=6V		5		V
V_{UV_VCC}	VCC UVLO threshold voltage	VCC falling edge		2.1		V
$V_{UV\_VCC\_HYS}$	VCC UVLO hysteresis voltage			0.1		V
I_{Q_VIN}	Standby current into VIN pin	VIN=EN=4V,VBUS=12V,FB=1.3V,no Ext.FET		48		uA
I_{Q_VBUS}	Standby current into VBUS pin	VIN=EN=4V,VBUS=12V,FB=1.3V,no Ext.FET		409		uA
I_{SD_VIN}	Shutdown current	EN=0V,VIN=4V(Input signal source)		14		uA
VBUS Section						
VBUS	VBUS operating range		4.5		24	V
V_{BUS_OVP}	VBUS OVP threshold voltage	Rising edge		25.2		V
V_{FB}	Reference voltage at FB pin			1.2		V
I_{FB}	FB pin leakage current	FB=1.2V	-50		50	nA
Error Amplifier Section						
G_M	Error amplifier trans-conductance	FB=1.2V, COMP=1.5V		640		uS
I_{COMP_source}	COMP pin source current			54		uA
I_{COMP_sink}	COMP pin sink current			54		uA
G_{CS}	COMP to current gain(Note4)			10		S
Power FET Section						
R_{ON_LS}	Low side NFET on-resistance	I_{DS}=0.5A		18		mΩ
R_{ON_HS}	High side NFET on-resistance	I_{DS}=0.5A		18		mΩ
I_{LK_LS}	Low side FET leakage current	V_{SW}=24V			1	uA
I_{LK_HS}	High side FET leakage current	V_{BUS}=24V, V_{SW}=0V			1	uA
VBST	High side driver supply voltage	BST-SW		5		V
ILIM Section						
V_{ILIM}	Reference voltage at ILIM			0.5		V
I_{ILIM}	Peak LS NFET current limit	R_{LIM}=100k, I_{limit}=1M/R_{SET}		10		A
		R_{LIM}=200k, I_{limit}=1M/R_{SET}		5		A
Frequency Section						
f_{sw}	Switching frequency	R_{FREQ}=300k,Fs=15x10^10/R_{FREQ}		500		kHz
t_{on_min}	Minimum LSFET on time(Note4)			105		ns

t_{off_min}	Minimum HSFET on time(Note4)			140		ns
EN Section						
V_{EN_H}	EN high threshold voltage	EN > V_{EN_H}, enable IC		1.2		V
V_{EN_L}	EN low threshold voltage	EN < V_{EN_L}, shutdown IC		1.0		V
I_{EN}	EN input current	V_{EN}=1.3V		541		nA
Short Circuit Protect Section						
I_{OCP}	LS NFET current threshold for OCP			15		A
I_{SCP}	LS NFET current threshold for SCP			20		A
V_{SCP}	FB voltage threshold for SCP			0.4		V
T_{HICCUP}	Waiting time for restart in hiccup mode			230		mS
Soft Start Section						
T_{PRO}	POR time			4		mS
T_{PRE_CHG}	VBUS Pre-charge time			4		mS
T_{TURN_ON}	Disconnect MOS Turn on time			4		mS
T_{START_UP}	FB Soft Startup time			4		mS
OTP Section						
T_{SD}	Thermal shutdown temperature			150		℃
T_{SD_HYS}	Thermal shutdown hysteresis temperature			20		℃

Note:
1) Guaranteed by design

8 Typical Characteristics

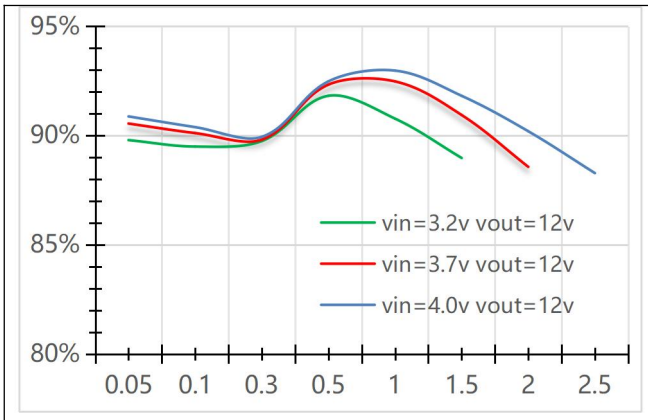


Fig. 8-1 Efficiency

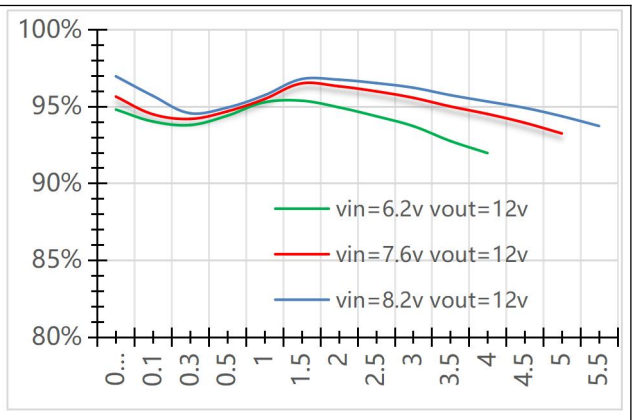
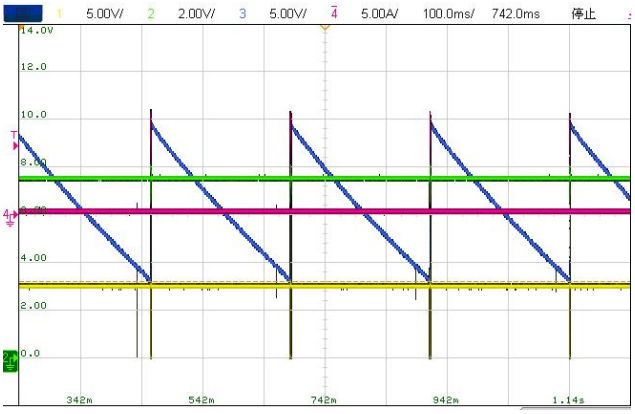


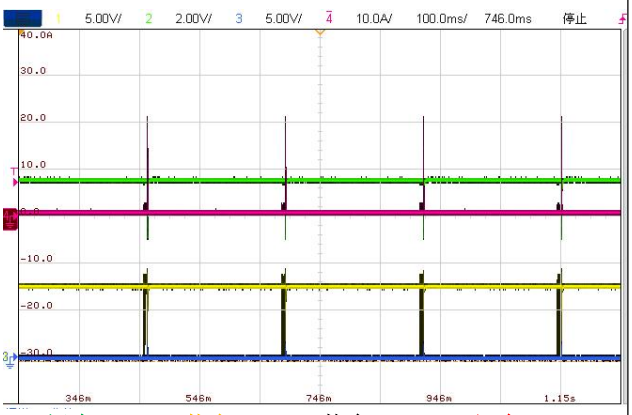
Fig. 8-2 Efficiency



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

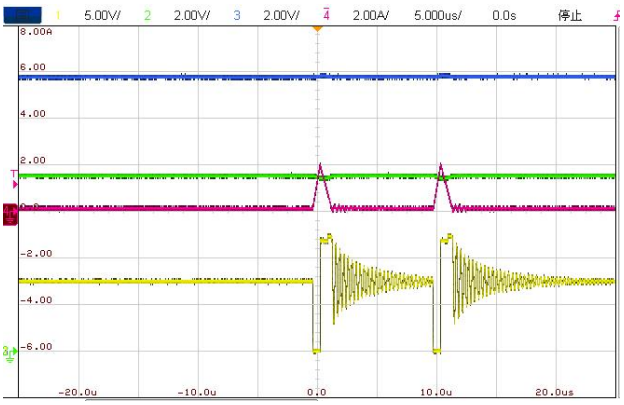
Fig.8-3 FB float OVP test



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

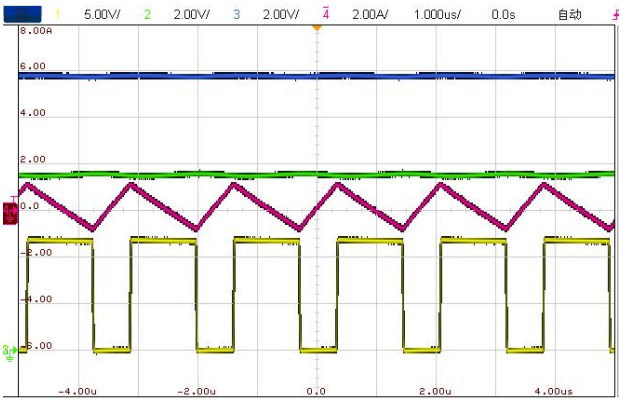
Fig.8-4 Short Circuit waveform



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

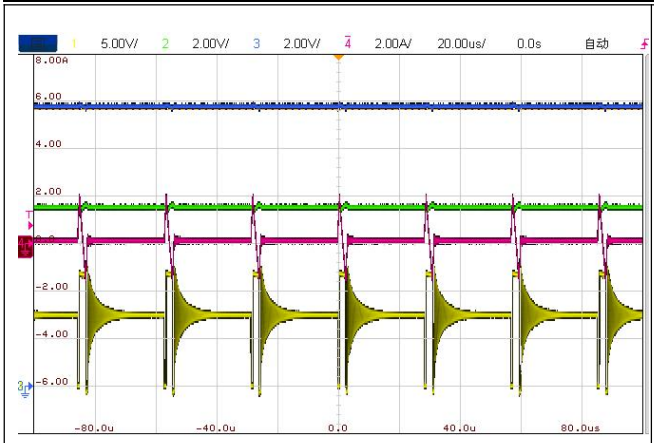
Fig.8-5 DCM Steady State waveform, Iout =0A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

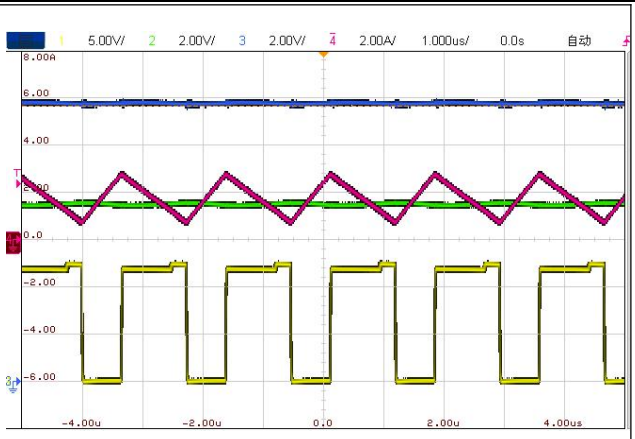
Fig.8-6 FCCM Steady State waveform, Iout =0A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

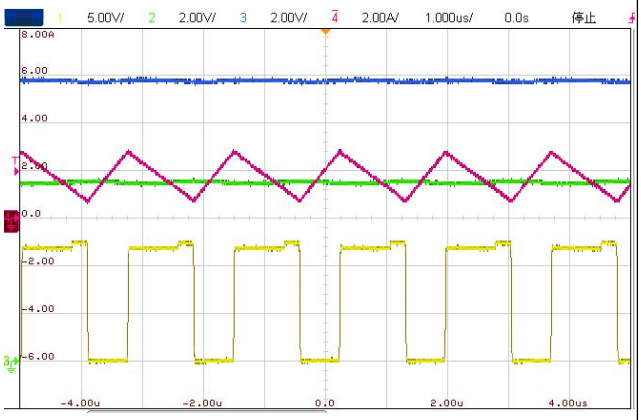
Fig.8-7 USM Steady State waveform, Iout =0A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

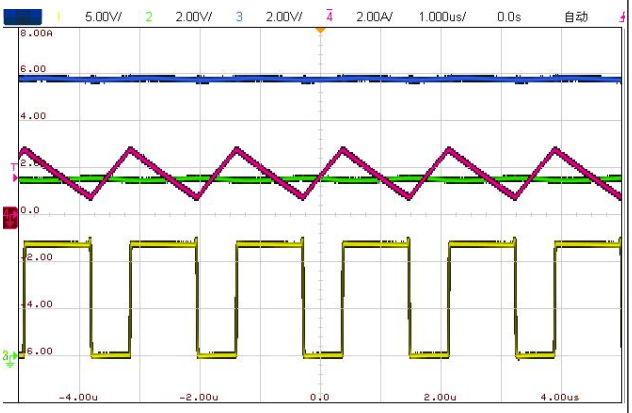
Fig.8-8 USM Steady State waveform, Iout =1A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

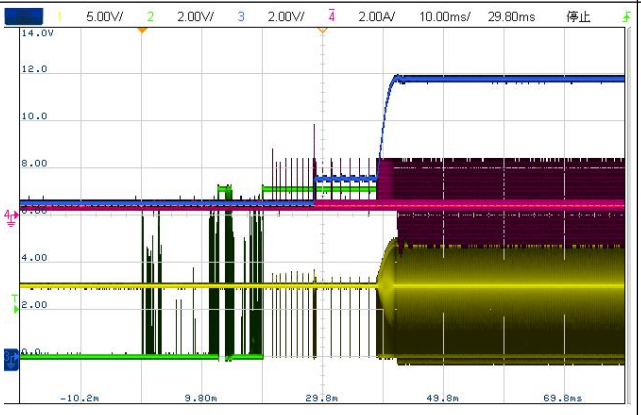
Fig.8-9 DCM Steady State waveform, Iout =1A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

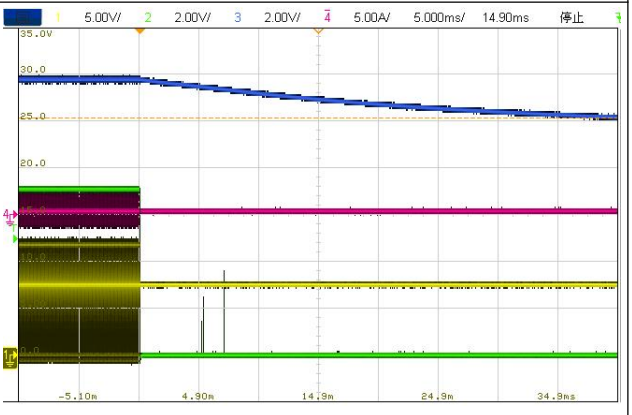
Fig.8-10 FCCM Steady State waveform, Iout =1A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

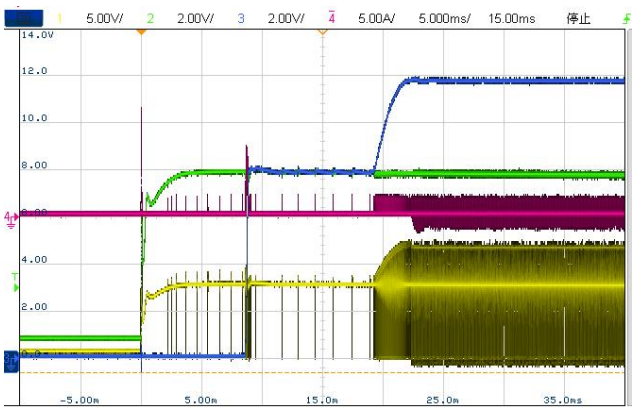
Fig.8-11 EN USM Start up waveform, Iout =0A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

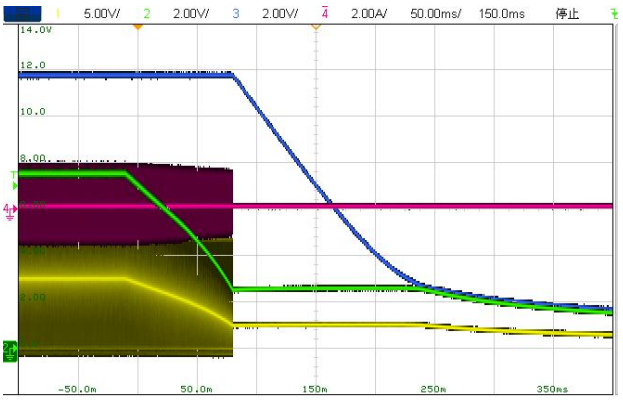
Fig.8-12 EN USM Shut down waveform, Iout =0A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

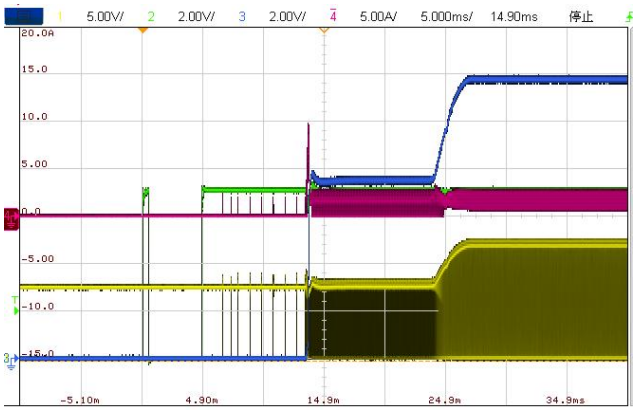
Fig.8-13 Vin USM Start up waveform, Iout =0A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

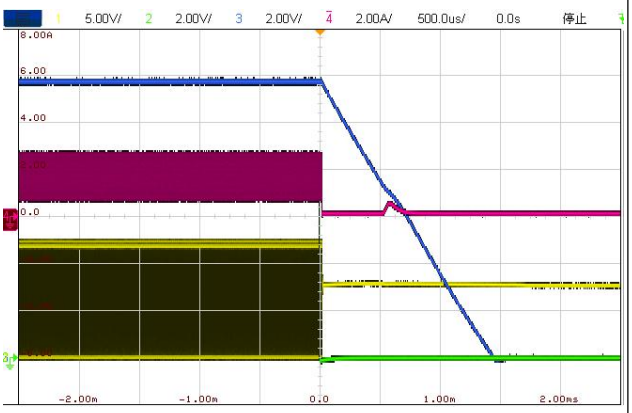
Fig.8-14 Vin USM Shut down waveform, Iout =0A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

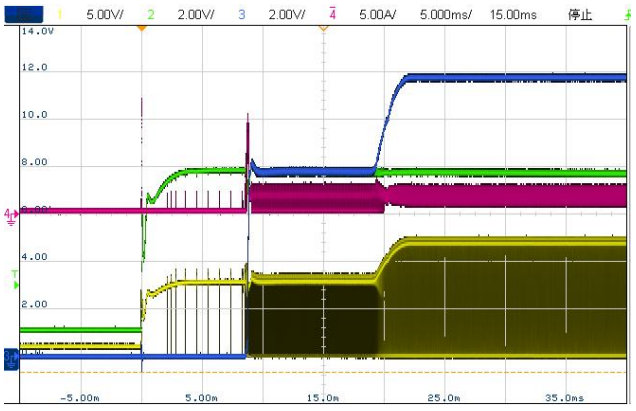
Fig.8-15 EN USM Start up waveform, Iout =1A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

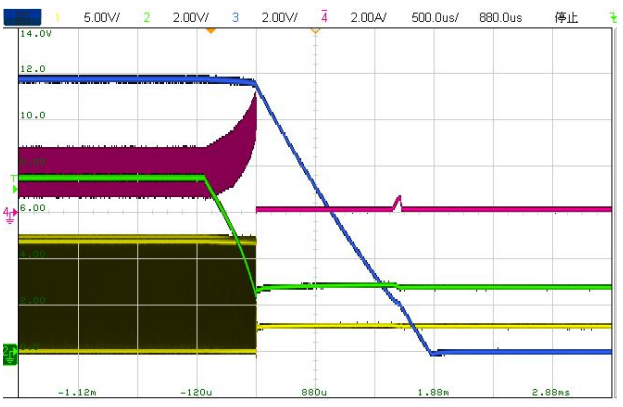
Fig.8-16 EN USM Shut down waveform, Iout =1A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

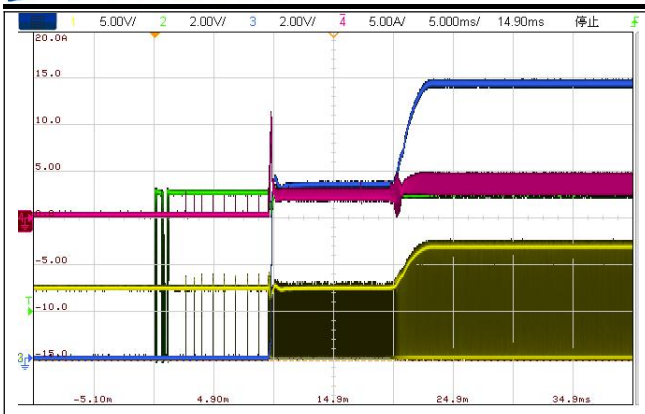
Fig.8-17 Vin USM Start up waveform, Iout =1A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

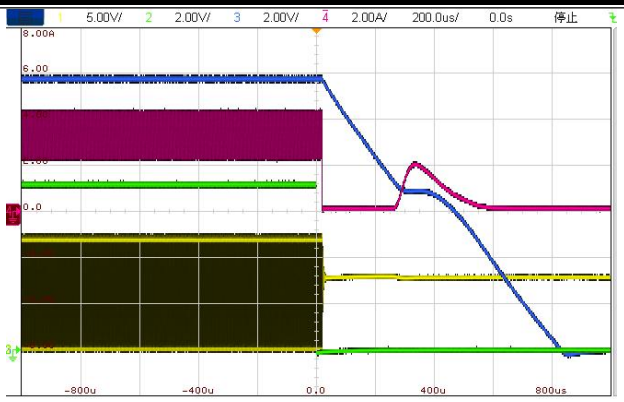
Fig.8-18 Vin USM Shut down waveform, Iout =1A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

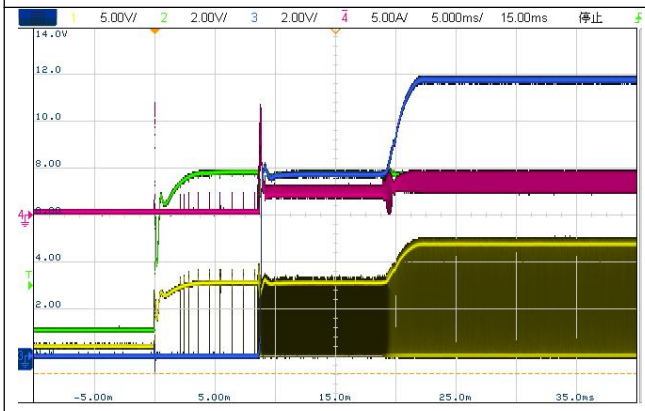
Fig.8-19 EN USM Start up waveform, Iout =2A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

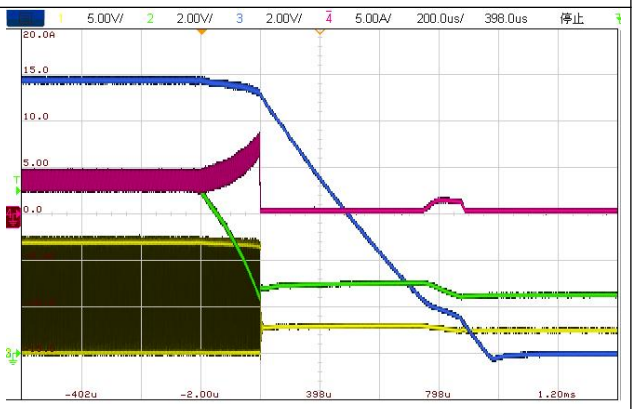
Fig.8-20 EN USM Shut down waveform, Iout =2A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

Fig.8-21 Vin USM Start up waveform, Iout =2A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=7.6V Vout=12V

Fig.8-22 Vin USM Shut down waveform, Iout =2A

9 Detailed Description

9.1 Overview

The PL32001 is a synchronous boost converter designed for delivering the switch peak current up to 15A and output voltage up to 20 V.

PL32001 has a mode selection function. When the MODE pin is left floating, the PL32001 enters USM mode. When the MODE pin is connected to VCC, the PL32001 enters CCM mode. When the MODE pin is grounded, the PL32001 enters DCM mode.

The PL32001 provides the excellent line and load transient response with the minimal output capacitor. The external loop compensation brings the flexibility to use a wider range of the inductor and output capacitor combinations.

PL32001 supports adjustable switching frequency from 33kHz to 2.2MHz.The device implements a programmable cycle-by-cycle current limit to protect the device from overload during the boost operation phase. The PL32001 triggers the hiccup short protection if the output current further increases and exceeds the short current threshold or the output voltage drops below the short threshold. And this device recovers automatically once the short condition releases.

Additionally, the PL32001 provides the gate driver for the external FET to isolate the output from input during shutdown.

9.2 Functional Block Diagram

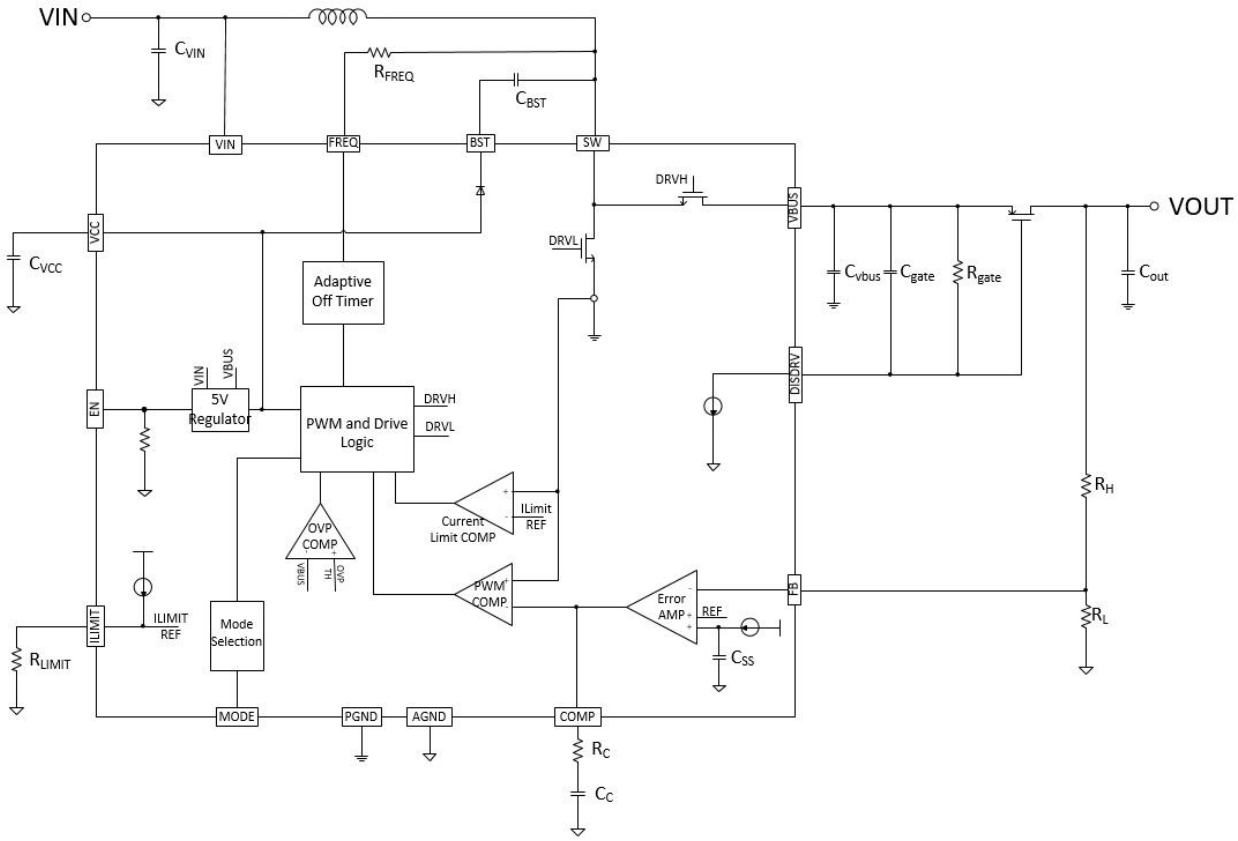


Fig. 9-2 Block Diagram

9.3 Feature Description

9.3.1 Under-voltage Lockout

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the UVLO threshold of 2.43V. A hysteresis of 270mV is added so that the device cannot be enabled again until the input voltage exceeds 2.7V. This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 2.43V and 2.7V.

9.3.2 Enable and Disable

When the input voltage is above UVLO rising threshold of 2.7V and the EN pin is pulled high above 1.2V, thePL32001 is enabled. When the EN pin is pulled below 1V, the PL32001 goes into the shutdown mode and stops switching.

9.3.3 Startup

When the input voltage to the device exceeds the UVLO threshold and EN pin pulled to high as well, thePL32001 starts to ramp up the output voltage. There is a switching pre-charge phase and the output voltage is charged up to input voltage (1.1 x VIN).
After the pre-charge phase ends (typical 4 ms), The PL32001 gradually turns on the external FET at the output side, which completely disconnects the output from the input during shutdown or output short happens.
After the turn-on phase ends (typical 4 ms), The PL32001 regulates the FB pin to the internal soft start voltage and results in a gradual rise of the output voltage starting from the input voltage level to the target output voltage. The soft start time is typical 4 ms, which helps the regulator to gradually reach the steady state setting point, thus reducing the startup stresses and surges.

9.3.4 Load Disconnect Gate Driver

The PL32001 device provides a DISDRV pin to drive the external FET at the output side, which completely disconnects the output from the input during shutdown or output short happens. During the device's start-up phase, the disconnect FET is controlled by the gate driver voltage of the external disconnect FET, there is an internal 55μA (typical) sink current. The load disconnect FET connection is shown as Figure 9-3-4.
The driver voltage and turn on / off timing can be set via the resistor and capacitor connecting between the DISDRV pin and the source of the external FET. See the Application and Implementation section for the details of how to select the gate resistor and capacitor.

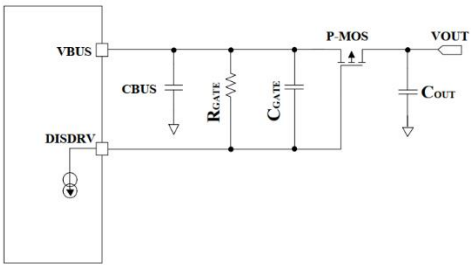


Fig. 9-3-4 Block Diagram

9.3.5 Adjustable Cycle-by-Cycle Switching Current Limit

When the PL32001 is in the normal boost switching phase, the device is prevented from the over current condition via the cycle by cycle current limit by sensing the current through the internal low-side FET. When the peak switch current triggers the current limit threshold, the low-side switch turns off to prevent the switching current further increasing.
The peak switch current limit can be set by a resistor connecting with the ILIMIT pin. The relationship between the current limit and the resistor is determined by Equation.

$$R_{LIMIT} = \frac{1000}{I_{LIMIT}}$$

Where R_{LIMIT} is the resistor for setting the current limit, with the unit of kΩ, I_{LIMIT} is switching peak current limit,with the unit of A. For instance, when the resistor value is 100kΩ, the switch peak current limit is 10 A.

9.3.6 Output Short Protection (with load disconnected FET)

In addition to the cycle-by-cycle current limiting, the PL32001 also has the output short protection. If the inductor current reaches the short protection limit threshold (typical 20A) or the output voltage drops below30%(typical) of the normal output voltage, the device enters into the hiccup protection mode. In the hiccup mode, the device shuts down itself and

restarts after 120ms (typical) waiting time which helps to reduce the total thermal dissipation. After the short condition releases, the device can recover automatically and restart the start-up phase.

9.3.7 Adjustable Switching Frequency

The PL32001 features of a wide adjustable switching frequency ranging up to 2.2MHz. The switching frequency is set by a resistor connected from SW to the FREQ pin.This pin cannot be left floating in the application.Use Equation to calculate the resistor value for a desired frequency.

$$\text{Freq} = \frac{150000}{R_{\text{Freq}}}\ \text{kHz}$$

Where R_{Freq} is the resistor for setting the frequency, with the unit of kΩ, Freq is switching frequency, with the unit of kHz. For instance, when the resistor value is 300kΩ, the switching frequency is 500kHz.

9.3.8 Mode selection

PL32001 has a mode selection function. When the MODE pin is grounded, the PL32001 operates in DCM mode, which is mainly selected for light loads. When the MODE pin is connected to VCC, the PL32001 works in CCM mode, which is mainly selected for heavy load. When the MODE pin is floating, the level of the MODE pin is at 1.2V (typical value), and the PL32001 works in the USM mode. In this mode, the system operating frequency will be limited to 33kHz~2.2MHz.

9.3.9 Error Amplifier

The PL32001 has a trans-conductance amplifier and compares the feedback voltage with the internal voltage reference (or the internal soft start voltage during startup phase). The trans-conductance of the error amplifiers 610μA/V typically. The loop compensation components are required to be placed between the COMP terminal and ground to balance the loop stability and the transient response time.

9.3.10 Start-up with the Output Pre-Biased

The PL32001 has been designed to prevent the low-side FET from discharging a pre-biased output. During the pre-biased startup, both high-side and low-side FETs are not allowed to be turned on until the internal soft start voltage is higher than the sensed output voltage at FB pin.

9.3.11 Bootstrap Voltage (BST)

The PL32001 has an integrated bootstrap regulator, and requires a small ceramic capacitor between the BST pin and SW pin to provide the gate drive voltage for the high-side FET. The bootstrap capacitor is charged when the BST-SW voltage is below regulation. The value of this ceramic capacitor should be above 100nF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics over temperature and DC biased voltage.

9.3.12 Over-voltage Protection

If the voltage at the VBUS pin is detected above over-voltage protection threshold, typically 24.9V, the PL32001 stops switching immediately until the voltage at the VBUS pin drops lower than the output over voltage protection threshold (with 300mV hysteresis). This function prevents the devices against the over-voltage and secures the circuits connected to the output from excessive over voltage.

9.3.13 Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to the excessive heat and power dissipation.Typically, the thermal shutdown occurs at the junction temperature exceeding 150°C. When the thermal shutdown is triggered, the device stops switching and recover when the junction temperature falls below130°C(typical).

9.4 Device Functional Modes

PL32001 operates at the adaptive constant off time peak current mode control (CMCOT). At the beginning of each switching cycle, the low-side FET switch turns on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. The PWM controller turns off the low-side FET when the peak inductor current reaches a threshold level set by the error amplifier output. After the low-side FET turns off, the high-side synchronous FET is turned on after a short dead time until the adaptive off timer end or until the inductor current reaches the reverse current sense threshold.

During the portion of the switching cycle when the low-side FET is on, the input voltage is applied across the inductor and stores the energy as the inductor current ramps up. Meanwhile only the output capacitor supplies the load current. When it turns off the low-side FET, the inductor transfers the stored energy via the high-side synchronous FET to replenish the output capacitor and also supply the load current. This operation repeats every switching cycle.

10 Application and Implementation

10.1 Setting the switching Frequency

The switching frequency of the PL32001 is set at 500kHz. Use Equation to calculate the required resistor value. For a target switching frequency of 500kHz, The calculated value is100kΩ.

10.2 Setting the Cycle-By-Cycle Current Limit

The current limit of the PL32001 could be programmed by an external resistor. Use Equation to calculate the required resistor value. For a target current limit of 10A, the calculated resistor value is 100kΩ.

10.3 Selecting the Inductor

There are several considerations in choosing this inductor.
1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{0.4 \times F_{SW} \times I_{OUT\_MAX}}$$

Where:

F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

PL32001 is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > \frac{V_{OUT}}{V_{IN}} \times I_{OUT\_MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve a good overall efficiency.

10.4 Selecting the Output Capacitors

The Boost Output capacitor C_{BD} and disconnection FET Output capacitor C_{OUT} are selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into account when selecting these capacitors. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 25V rating and more than 22uF capacitors.

10.5 Selecting the Input Capacitors

Multi layer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 22μF input capacitor is sufficient for the most applications, larger values maybe used to reduce input current ripple.
Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, should be placed between CIN and the power source lead to reduce ringing that can occur between the inductance of the power source leads and CIN.

10.6 Selecting the Disconnect FET

The PL32001 provides a gate driver to control an external FET to disconnect the output from the input at shutdown or output short conditions.
The V_{DS}, I_{DS} and safe operation area (SOA) should be taken into consideration when selecting the FET:

- The drain-to-source voltage rating should be higher than the output max. voltage, $V_{DS\_DIS\_MAX} = V_{OUT}$,
- The drain-to-source RMS current rating is the maximum output current. $I_{DS\_DIS\_RMS} = I_{OUT}$,
- The SOA should be considered when the output short occurs, and there is heat caused by the short protection response time and surge current, SOA > QSHORT.

$$Q_{SHORT} = 0.5 \times V_{OUT} \times I_{SHORT} \times T_{SHORT}$$

where

- $V_{DS\_DIS\_MAX}$ is the maximum drain-source voltage
- I_{DS_DIS} is the drain-source RMS current
- I_{SHORT} is the short current
- T_{SHORT} is the response time before the short protection triggered
- Q_{SHORT} is the heat produced for the output short

For instance: V_{OUT} = 16 V, I_{SHORT} = 20 A , T_{SHORT} = 30μs. SOA ≥ 4.8mJ, $V_{DS\_DIS\_MAX}$ ≥ 16 V.

An additional capacitor between the gate and source of the external FET is required to slow the turn-on speed.

$$T_{ON\_PFET} = \frac{V_{TH\_PFET} \times C_{GS\_PFET}}{I_{DIS\_PFET}}$$

where

- T_{ON_PFET} is the on time of external FET
- V_{TH_PFET} is the gate threshold of external FET
- C_{GS_PFET} is the total gate capacitance of connected between gate and source external FET. (including the gate-source capacitance of the FET)
- I_{DIS_PFET} is the discharge current inside of PL32001, it is 55μA typically

Given 1.5 V threshold, C_{GS_PFET} is 10nF, the T_{ON_PFET} is around 300μs.Please be aware that the maximum turn on time should not exceed 4ms, and the maximum capacitance C_{GS_PFET} should be < 100nF. Otherwise,the PL32001 could not startup normally if the disconnect FET could not be turn on within the 4ms.
The gate resistor depends on the gate-source voltage of the external FET,

$$R_{GATE} = \frac{V_{GATE}}{I_{DIS\_PFET}}$$

Given the 5V V_{GATE}, the R_{GATE} = 100kΩ

10.7 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during each cycle's turn-on and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 100nF to 1μF. C_{BST} should be a good quality, low ESR,ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 100nF was selected for this design example.

10.8 Selecting the VCC Capacitor

The primary purpose of the VCC capacitor is to supply the peak transient currents of the driver and bootstrap capacitor as well as provide stability for the VCC regulator. The value of C_{VCC} should be at least 10 times greater than the value of C_{BST}, and should be a good quality, low ESR, ceramic capacitor. C_{VCC} should be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 4.7μF was selected for this design example.

11 PCB Layout

11.1 Guideline

The basic PCB board layout requires a separation of sensitive signal and power paths. If the layout is not carefully done, the regulator could suffer from the instability or noise problems.The checklist below is suggested that be followed to get good performance for a well-designed board:

1. Minimize the high current path including the switch FET, rectifier FET, and the output capacitor. This loop contains high di/dt switching currents and easy to transduce the high frequency noise;

2. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize inter plane coupling;

3. Use a combination of bulk capacitors and smaller ceramic capacitors with low series resistance for the input and output capacitors. Place the smaller capacitors closer to the IC to provide a low impedance path for decoupling the noise;

4. The ground area near the IC must provide adequate heat dissipating area. Connect the wide power bus (e.g., VOUT, SW , GND) to the large area of copper, or to the bottom or internal layer ground plane, using vias for enhanced thermal dissipation;

5. Place the input capacitor being close to the VIN pin and the PGND pin in order to reduce the input supply ripple;

5. Place the noise sensitive network like the feedback and compensation being far away from the SW trace;

7. Use a separate ground trace to connect the feedback, compensation, frequency set, and the current limit set circuitry. Connect this ground trace to the main power ground at a single point to minimize circulating currents.

11.2 Application Examples

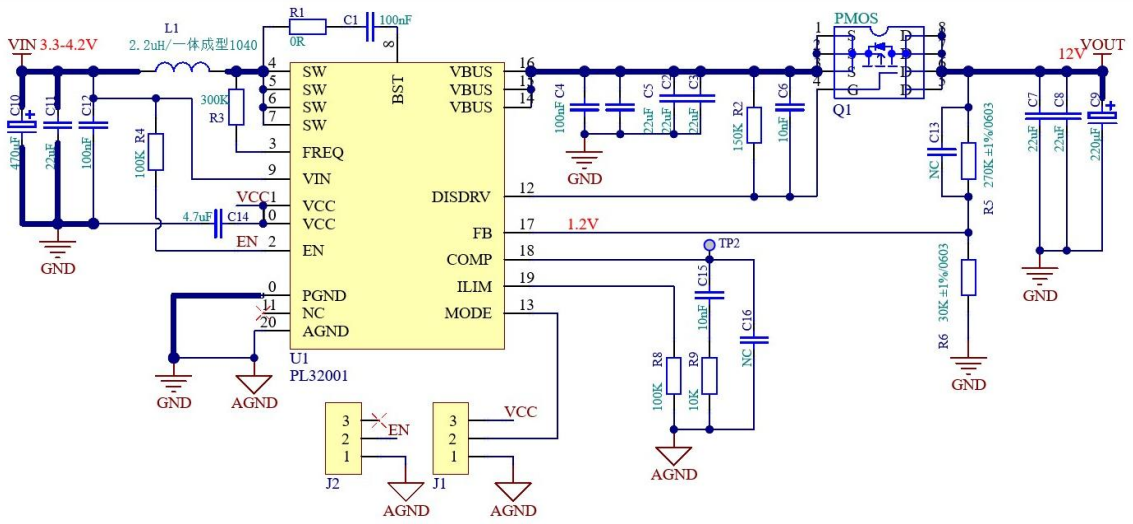


Fig. 11-2-1 Schematic

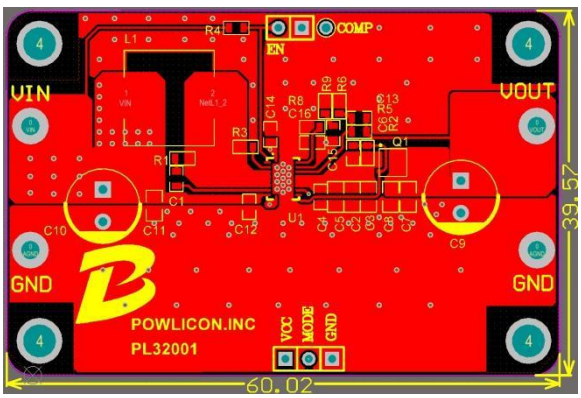


Fig. 11-2-2 Top Layer

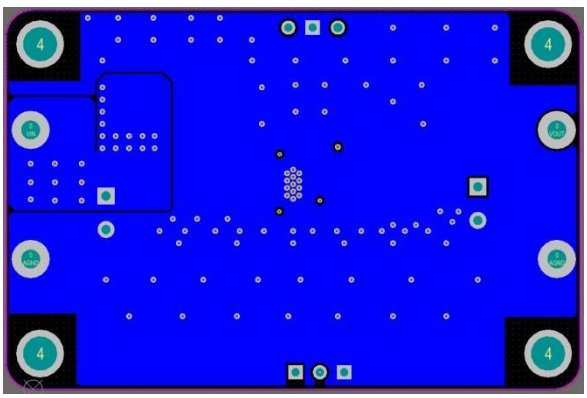
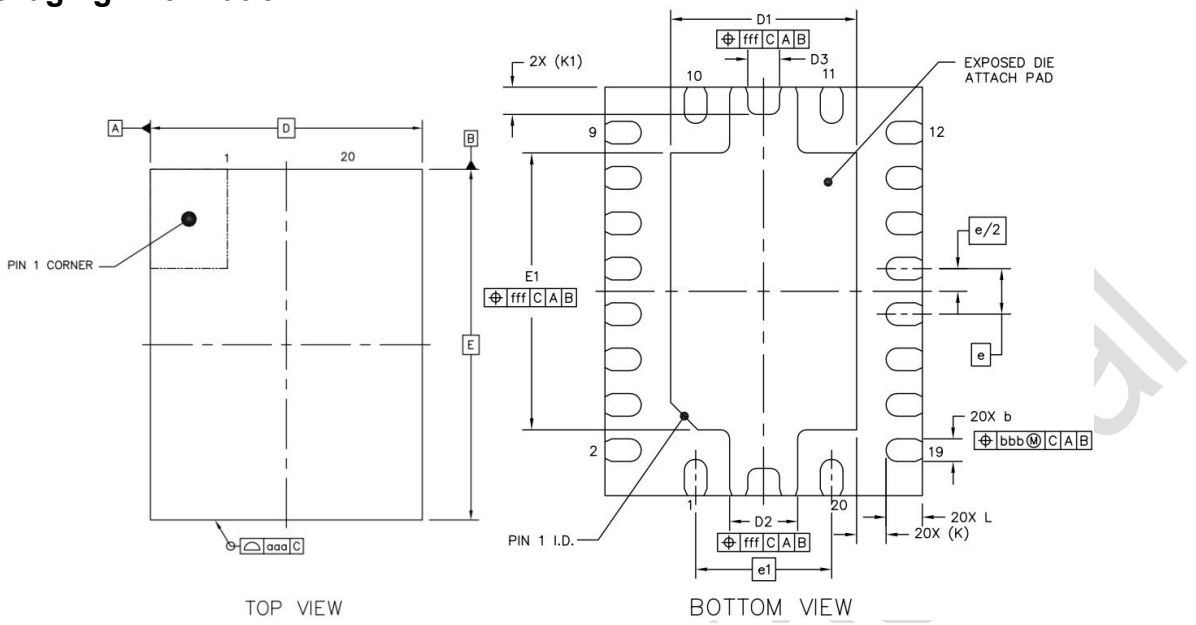
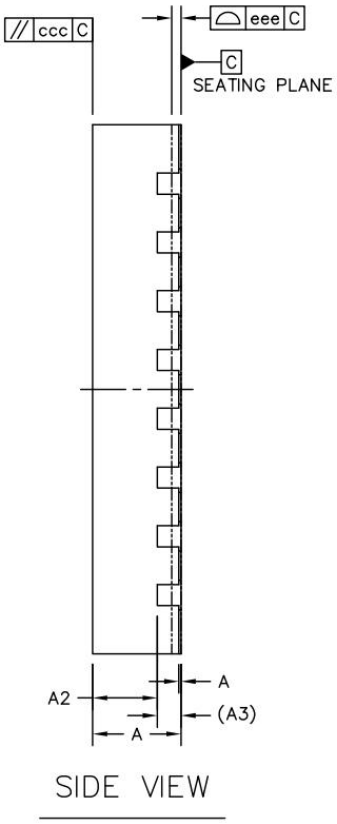


Fig. 11-2-3 Bottom Lay

12 Packaging Information





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3.5 BSC	
	Y	E		4.5 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD PITCH		e1		1.5 BSC	
EP SIZE	X	D1	1.95	2.05	2.15
	Y	E1	2.95	3.05	3.15
	X	D2	0.65	0.75	0.85
EP EDGE TO EP EDGE		D3	0.25	0.35	0.45
LEAD LENGTH		L	0.3	0.4	0.5
EP EDGE TO PACKAGE EDGE		K1	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K		0.325 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	