PL59201 100V Synchronous Buck Controller

1 Features

- Versatile Synchronous Buck DC-DC Controller
  Wide Input Voltage Range of 6 V to 100 V
  Adjustable Output Voltage From 0.8 V to 60 V
- Meets EN55022 / CISPR 22 EMI Standards
  Lossless $R_{DS(on)}$ or Shunt Current Sensing
- Switching Frequency From 100 kHz to 1 MHz
  SYNCIn and SYNCOut Capability
- 0.8V Reference With ±1% Feedback Accuracy
- 7.5V Gate Drivers for Standard VTH MOSFETs
- 30ns Adaptive Dead-Time Control
- 2.3A Source and 3.5A Sink Capability
- Low-Side Soft-Start for Prebiased Start-Up
- Adjustable Soft-Start or Optional Voltage Tracking
- Fast Line and Load Transient Response
  Voltage-Mode Control With Line Feed forward
  High Gain-Bandwidth Error Amplifier
- Precision Enable Input and Open-Drain Power Good Indicator for Sequencing and Control
- Inherent Protection Features for Robust Design
- Hiccup Mode Over Current Protection
- Input UVLO With Hysteresis
- VCC and Gate Drive UVLO Protection
- Thermal Shutdown Protection With Hysteresis
- QFN3.5X4.5-20L

2 Applications

- Remote Radio Unit (RRU) and BTS
- Networking and Computing Power
- Non-Isolated PoE and IP Cameras
- Industrial Motor Drives

3 Description

The PL59201 is a 100V synchronous buck controller is designed to regulate from a high input voltage source or from an input rail subject to high voltage transients, minimizing the need for external surge suppression components. The PL59201 continues to operate during input voltage dips as low as 6V, at nearly 100% duty cycle if needed, making it well suited for industrial control, robotic, datacom, and RF power amplifier applications.

Forced-PWM (FPWM) operation eliminates frequency variation to minimize EMI, while a user-selectable diode emulation feature lowers current consumption at light-load conditions. Cycle-by-cycle over current protection is accomplished by measuring the voltage drop across the low-side MOSFET or by using an optional current sense resistor. The adjustable switching frequency as high as 1 MHz can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications.

4 Typical Application Schematic

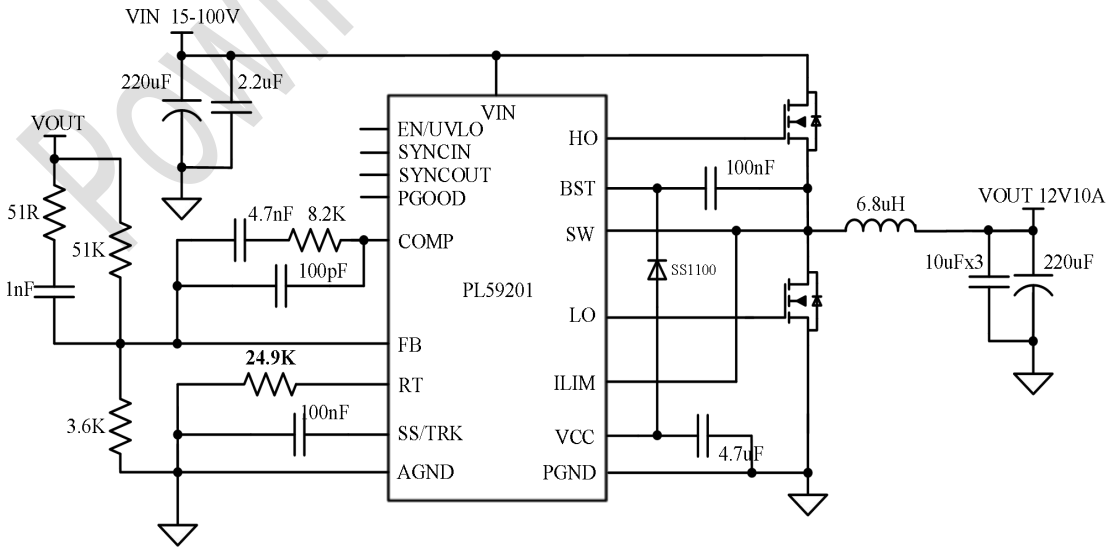


Fig.1 Typical Application Schematic

5 Pin Configuration and Functions

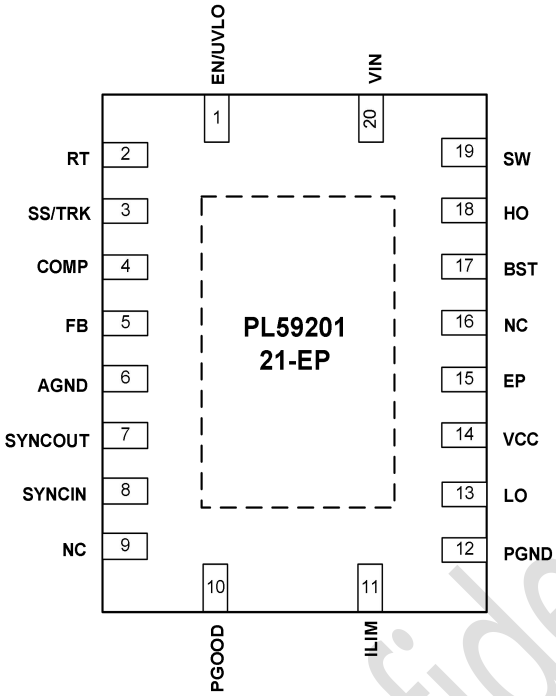


Fig.2 Pin-Function(QFN3.5X4.5-20L)

Pin		Description
Number	Name	
1	EN/UVLO	Enable pin.
2	RT	Oscillator frequency adjust pin. The internal oscillator is programmed with a single resistor between RT and the AGND. Recommends a maximum oscillator frequency of 1 MHz. An RT pin resistor is required even when using the SYNCIN pin to synchronize to an external clock.
3	SS/TRK	Soft-start and voltage-tracking pin. An external capacitor and an internal 10μA current source set the ramp rate of the error amplifier reference during start-up. When the SS/TRK pin voltage is less than 0.8V, the SS/TRK voltage controls the non-inverting input of the error amp. When the SS/TRK voltage exceeds 0.8V, the amplifier is controlled by the internal 0.8V reference. SS/TRK is discharged to ground during standby and fault conditions. After start-up, the SS/TRK voltage is clamped 115mV above the FB pin voltage. If FB falls due to a load fault, SS/TRK is discharged to a level 115mV above FB to provide a controlled recovery when the fault is removed. Voltage tracking can be implemented by connecting a low impedance reference between 0V and 0.8V to the SS/TRK pin. The 10μA SS/TRK charging current flows into the reference and produces a voltage error if the impedance is not low. Connect a minimum capacitance from SS/TRK to AGND of 2.2nF.
4	COMP	Low impedance output of the internal error amplifier. Connect the loop compensation network between the COMP pin and the FB pin.
5	FB	Feedback connection to the inverting input of the internal error amplifier. A resistor divider from the output to this pin sets the output voltage level. The regulation threshold at the FB pin is nominally 0.8V.
6	AGND	Analog ground. Return for the internal 0.8V voltage reference and analog circuits.
7	SYNCOUT	Synchronization output. Logic output that provides a clock signal that is 180° out-of-phase with the high- side FET gate drive. Connect SYNCOUT of the master PL59201 to the SYNCIN pin of a second PL59201 to operate two controllers at the same frequency with 180° interleaved high-side FET switch turn-on transitions. Note that the SYNCOUT pin does not provide 180° interleaving when the controller is operating from an external clock that is different from the free-running frequency set by the RT resistor.

8	SYNCIN	Dual function pin for providing an optional clock input and for enabling diode emulation by the low-side MOSFET. Connecting a clock signal to the SYNCIN pin synchronizes switching to the external clock. Diode emulation by the low-side MOSFET is disabled when the controller is synchronized to an external clock, and negative inductor current can flow in the low-side MOSFET with light loads. A continuous logic low state at the SYNCIN pin enables diode emulation to prevent reverse current flow in the inductor. Diode emulation results in discontinuous mode operation (DCM) at light loads, which improves efficiency. A logic high state at the SYNCIN pin disables diode emulation producing forced-PWM (FPWM) operation. During soft-start when SYNCIN is high or a clock signal is present, the PL59201 operates in diode emulation mode until the output is in regulation, then gradually increases the SW zero-cross threshold, resulting in a gradual transition from DCM to FPWM.
9	NC	This pin is floating, do not have electrical connections.
10	PGOOD	Power Good indicator. This pin is an open-drain output. A high state indicates that the voltage at the FB pin is within a specified tolerance window centered at 0.8V.
11	ILIM	Current limit adjust and current sense comparator input. A current sourced from the ILIM pin through an external resistor programs the threshold voltage for valley current limiting. The opposite end of the threshold adjust resistor can be connected to either the drain of the low-side MOSFET for RDS(on) sensing or to a current sense resistor connected to the source of the low-side FET.
12	PGND	Power ground return pin for the low-side MOSFET gate driver. Connect directly to the source of the low- side MOSFET or the ground side of a shunt resistor.
13	LO	Low-side MOSFET gate drive output.
14	VCC	Output of the 7.5V bias regulator. Locally decouple to PGND using a low ESR/ESL capacitor located as close as possible to the controller.
15	EP	Pin internally connected to exposed pad of the package. Electrically isolated.
16	NC	No electrical connection.
17	BST	Bootstrap supply for the high-side gate driver. Connect to the bootstrap (boot) capacitor. The bootstrap capacitor supplies current to the high-side FET gate and must be placed as close as possible to controller. Use an external Schottky diode to charge the bootstrap capacitor, connect the cathode of the diode to the BST pin and anode to VCC.
18	HO	High-side MOSFET gate drive output.
19	SW	Switching node of the buck controller.
20	VIN	Supply voltage input for the VCC LDO regulator.
21	EP	Exposed pad of the package. Electrically isolated. Solder to the system ground plane to reduce thermal resistance.

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking	MSL
PL59201	**PL59201IQN20A**	**QFN3.5X4.5-20L**	**4000**	**59201 RAAYMD**	**3**

59201: Part Number
RAAYMD : RAA: LOT NO.; YMD: Package Date Code

7 Specifications

7.1 Absolute Maximum Ratings(Note1)

PARAMETER	MIN	MAX	Unit
VIN	–0.3	100	V
SW	–1	100	
SW (20ns transient)	–5	100	
ILIM	0	100	
EN/UVLO	–0.3	100	
VCC,PGOOD,SYNCIN	–0.3	14	
FB, COMP, SS/TRK, RT	–0.3	6	
BST	–0.3	110	
BST to VCC		105	
BST to SW	–0.3	14	
VCC to BST (20ns transient)		7	
LO (20ns transient)	–3		

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
TST	Storage Temperature Range	-65	+150	°C
TJ	Junction Temperature	-40	+150	°C
VESD	HBM Human body model	2		kV

7.3 Recommended Operating Conditions (Note 2)

PARAMETER	MIN	MAX	Unit
VIN	5.5	100	V
SW	–1	100	
ILIM	0	100	
External VCC bias rail	8	13	
EN/UVLO	–0.3	100	
BST	–0.3	110	
BST to VCC		100	
BST to SW	5	13	
PGOOD		13	
SYNCOUT	–1	1	mA
PGOOD		2	
Tj	–40	150	°C

7.4 Thermal Information(Note 3)

Symbol	Description	QFN3.5X4.5-20L	Unit
θ_{JA}	Junction to ambient thermal resistance	36.8	°C/W
θ_{JC}	Junction to case thermal resistance	28	

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1” square of 1 oz copper.

7.5 Electrical Characteristics

Typical values correspond to TJ = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated. VIN = 48 V, VEN/UVLO = 1.5 V, RRT = 25 kΩ unless otherwise stated.(1)(2)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
VIN	Operating input voltage range	IVCC ≤ 10 mA at VVIN = 5.5 V	5.5		100	V
IQ-RUN	Operating input current, not switching	VEN/UVLO = 1.5 V, VSS/TRK = 0 V		1.8		mA
IQ-STBY	Standby input current	VEN/UVLO = 1 V		1.75		mA
IQ-SDN	Shutdown input current	VEN/UVLO = 0 V, VVCC < 1 V		15		μA
VCC REGULATOR						
VVCC	VCC regulation voltage	VSS/TRK = 0 V, 9 V ≤ VVIN ≤ 100 V, 0 mA < IVCC ≤ 20 mA		7.5		V
VVCC-LDO	VIN to VCC dropout voltage	VVIN = 6 V, VSS/TRK = 0 V, IVCC = 20 mA		0.25		V
ISC-LDO	VCC short-circuit current	VSS/TRK = 0 V, VVCC = 0 V		50		mA
VVCC-UV	VCC under voltage threshold	VVCC rising		4.93		V
VVCC-UVH	VCC under voltage hysteresis	Rising threshold – falling threshold		0.26		V
VVCC-EXT	Minimum external bias supply voltage	Voltage required to disable VCC regulator	8			V
IVCC	External VCC input current, not switching	VSS/TRK = 0 V, VVCC = 13 V			2.3	mA
ENABLE AND INPUT UVLO						
VEN	Shutdown to operating threshold			1.2		V
IEN-HYS	Shutdown to operating hysteresis			0.2		V
ERROR AMPLIFIER						
VREF	FB reference voltage	FB connected to COMP		800		mV
VCOMP-OH	COMP output high voltage	VFB = 0 V, COMP sourcing 1 mA		5		V
VCOMP-OL	COMP output low voltage	COMP sinking 1 mA			0.3	V
SOFT-START AND VOLTAGE TRACKING						
ISS	SS/TRK capacitor charging current	VSS/TRK = 0 V		10		μA
POWER GOOD INDICATOR						

PGUTH	FB upper threshold for PGOOD high to low	% of VREF, VFB rising	107.5 %	
PGLTH	FB lower threshold for PGOOD high to low	% of VREF, VFB falling	92.5 %	
TPG-RISE	PGOOD rising filter	FB to PGOOD rising edge	25	μs
TPG-FALL	PGOOD falling filter	FB to PGOOD falling edge	25	μs
VPG-OL	PGOOD low state output voltage	VFB = 0.9 V, IPGOOD = 2 mA	150	mV
IPG-OH	PGOOD high state leakage current	VFB = 0.8 V, VPGOOD = 13 V	400	nA
OSCILLATOR				
FSW1	Oscillator Frequency – 1	RRT = 100 kΩ	100	kHz
FSW2	Oscillator Frequency – 2	RRT = 25 kΩ	400	kHz
SYNCHRONIZATION INPUT AND OUTPUT				
FSYNC	SYNCIN external clock frequency range	% of nominal frequency set by RRT	–20% +50 %	
VSYNC-IH	Minimum SYNCIN input logic high		2	V
VSYNC-IL	Maximum SYNCIN input logic low		0.4	V
RSYNCIN	SYNCIN input resistance	VSYNCIN = 3 V	20	kΩ
tSYNCI-PW	SYNCIN input minimum pulse width	Minimum high state or low state duration	50	ns
VSYNCO-OH	SYNCOUT high state output voltage	ISYNCOUT = –1 mA (sourcing)	3	V
VSYNCO-OL	SYNCOUT low state output voltage	ISYNCOUT = 1 mA (sinking)	0.4	V
tSYNCOUT	Delay from HO rising to SYNCOUT leading edge	VSYNCIN = 0 V, TS = 1/FSW, FSW set by RRT	TS/2 – 140	ns
tSYNCIN	Delay from SYNCIN leading edge to HO rising	50% to 50%	180	ns
BOOTSTRAP DIODE AND UNDERVOLTAGE THRESHOLD				
VBST-UV	BST to SW under voltage detection	VBST – VSW falling	4.2	V
VBST-HYS	BST to SW under voltage hysteresis	VBST – VSW rising	0.3	V
PWM CONTROL				
tON(MIN)	Minimum controllable on-time	VBST – VSW = 7 V, HO 50% to	110	ns

		50%				
tOFF(MIN)	Minimum off-time	VBST – VSW = 7 V, HO 50% to 50%		140		ns
Dmax	Maximum duty cycle	Fsw=100kHz		98%		
OVERCURRENT PROTECT (OCP) – VALLEY CURRENT LIMITING						
IRS	ILIM source current, RSENSE mode	Low voltage detected at ILIM	90	100	100	µA
IRDSON	ILIM source current, RDS(on) mode	SW voltage detected at ILIM, TJ = 25°C	180	200	220	µA
VILIM-TH	ILIM comparator threshold at ILIM		–8	–2	3.5	mV
HICCUP MODE FAULT PROTECTION						
CHICC-DEL	Hiccup mode activation delay	Clock cycles with current limiting before hiccup off-time activated		128		cycles
CHICCUP	Hiccup mode off-time after activation	Clock cycles with no switching followed by SS/TRK release		8192		cycles
GATE DRIVERS						
HDRV	Peak HDRV Source Current			2.3		A
	Peak HDRV Sink Current			3.5		A
LDRV	Peak LDRV Source Current			2.3		A
	Peak LDRV Sink Current			3.5		A
Tr(HDRV)	CLOAD = 1000pF			5.5		ns
Tf(HDRV)	CLOAD = 1000pF			3.5		ns
Tr(LDRV)	CLOAD = 1000pF			5.5		ns
Tf(LDRV)	CLOAD = 1000pF			3.5		ns
Tdelay1	Top Gate Off to Bottom Gate On Delay			30		ns
Tdelay2	Bottom Gate Off to Top Gate On Delay			30		ns
THERMAL SHUTDOWN						
TSD	Thermal shutdown threshold	TJ rising		150		°C
TSD-HYS	Thermal shutdown hysteresis		15			°C

Note 1: All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 2: The junction temperature (TJ in °C) is calculated from the ambient temperature (TA in °C) and power dissipation (PD in Watts) as follows: TJ = TA + (PD • RθJA) where RθJA (in °C/W) is the package thermal impedance provided in 7.4.

8 Typical Characteristics

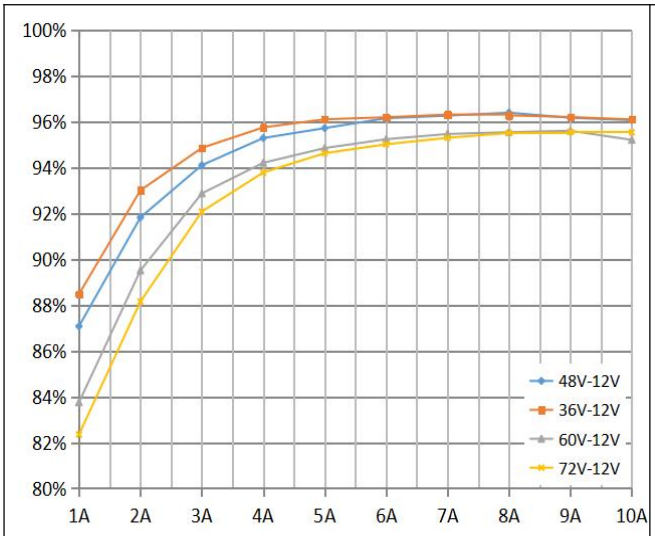


Fig8-1 Efficiency-Vout:12V/1-10A

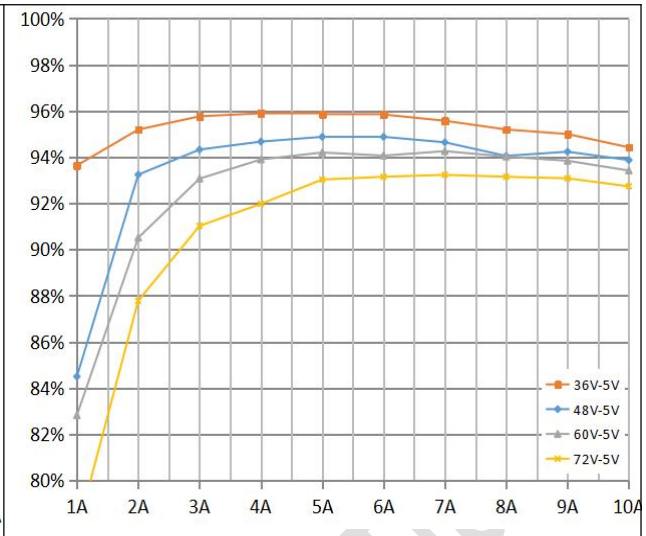
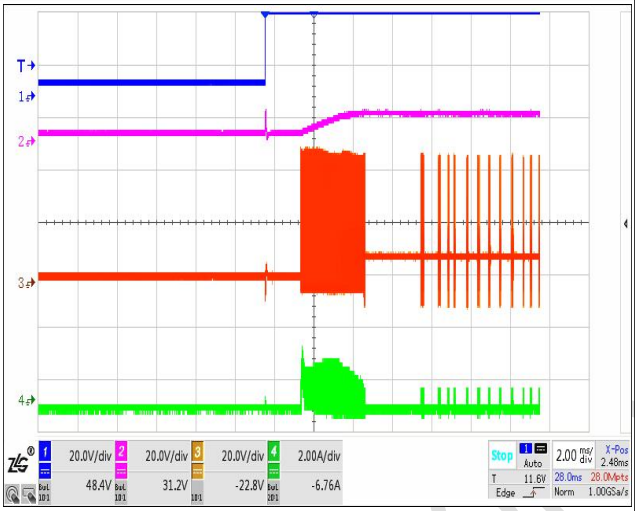
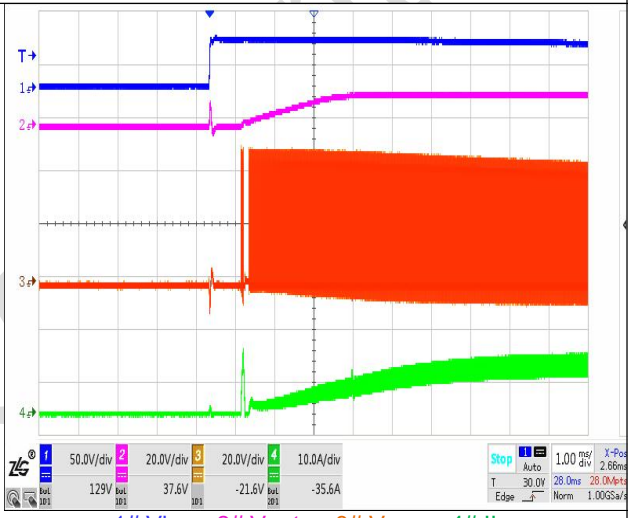


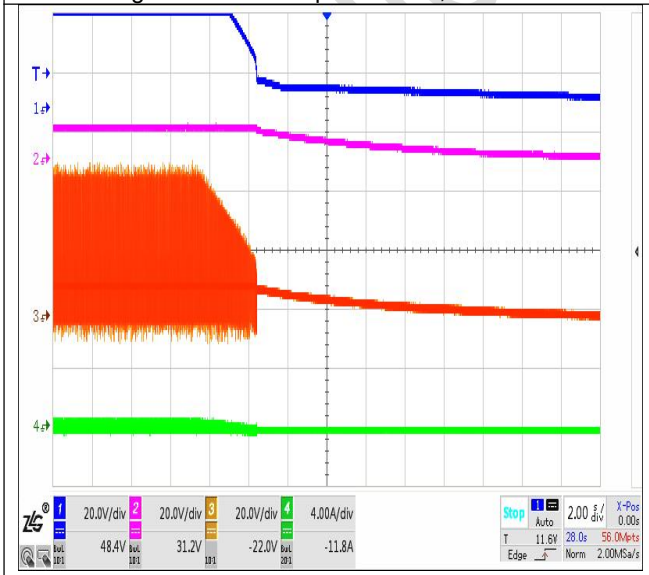
Fig8-2 Efficiency-Vout:5V/1-10A EXTVCC=9V



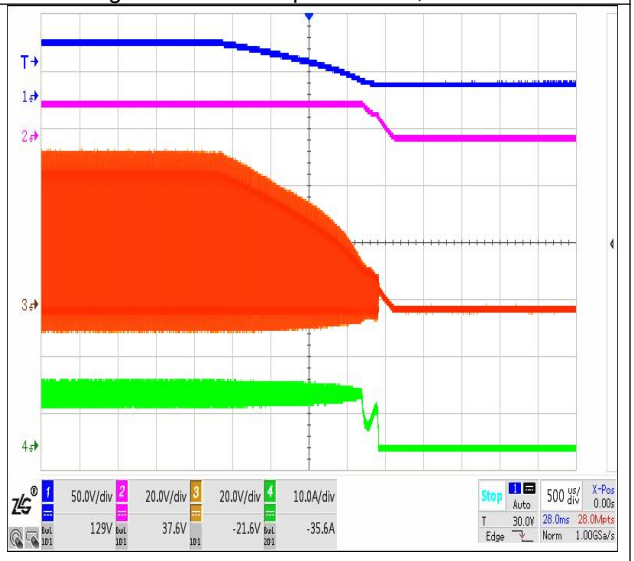
1#:Vin 2#:Vout 3#:Vsw 4#:IL
Vin=48V Vout=12V
Fig8-3 Vin Start up waveform, Iout =0A



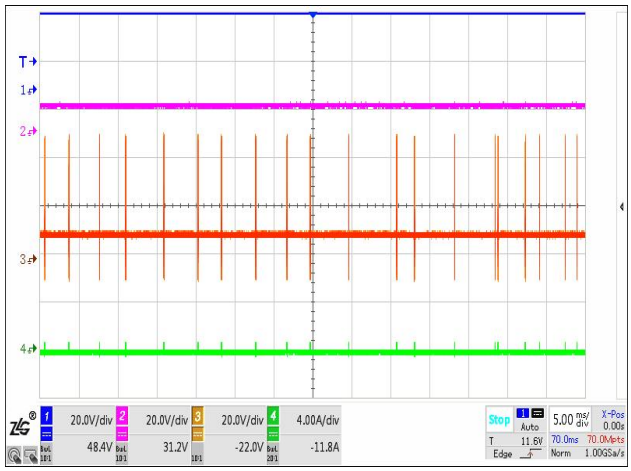
1#:Vin 2#:Vout 3#:Vsw 4#:IL
Vin=48V Vout=12V
Fig8-4 Vin Start up waveform, Iout =10A



1#:Vin 2#:Vout 3#:Vsw 4#:IL
Vin=48V Vout=12V
Fig8-5 Vin Shut down waveform, Iout =0A



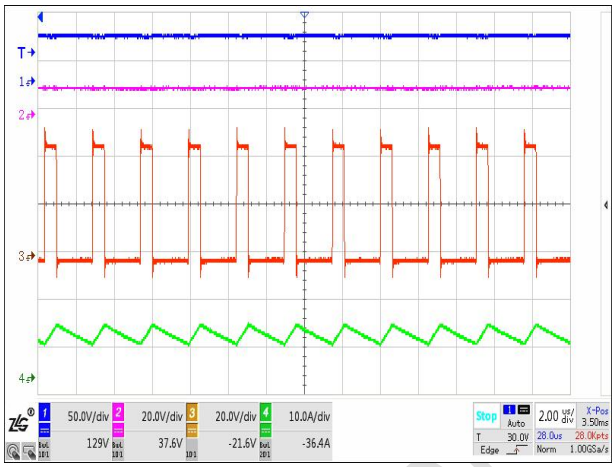
1#:Vin 2#:Vout 3#:Vsw 4#:IL
Vin=48V Vout=12V
Fig8-6 Vin Shut down waveform, Iout =10A



1#:Vin 2#:Vout 3#:Vsw 4#:IL

Vin=48V Vout=12V

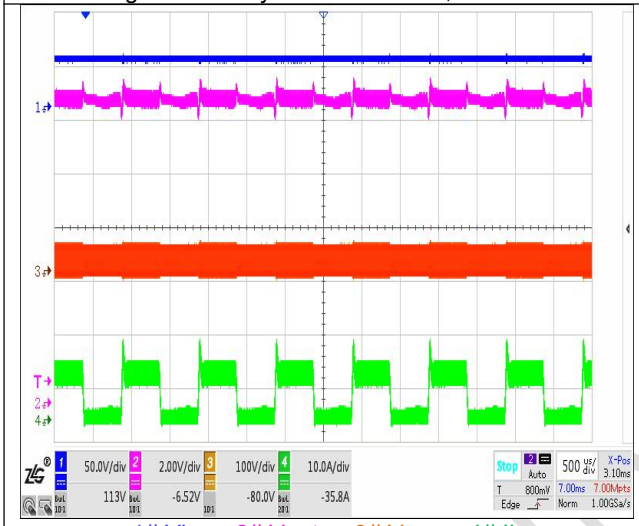
Fig8-7 Steady State waveform, Iout =0A



1#:Vin 2#:Vout 3#:Vsw 4#:IL

Vin=48V Vout=12V

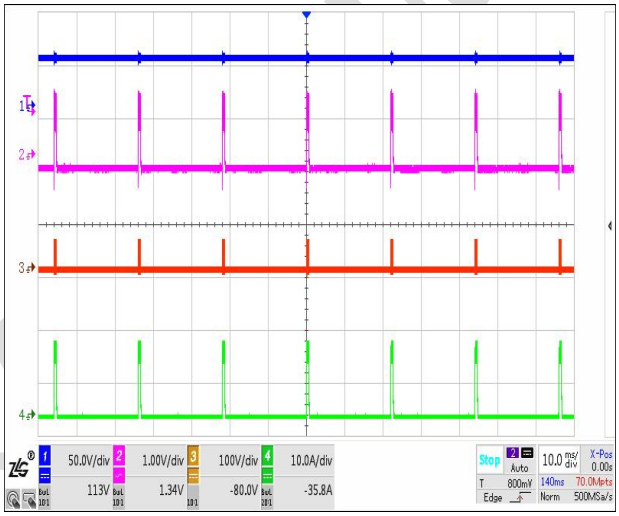
Fig8-8 Steady State waveform, Iout =10A



1#:Vin 2#:Vout 3#:Vsw 4#:IL

Vin=48V Vout=12V/1-9A

Fig8-9 Load Translent Ripple



1#:Vin 2#:Vout 3#:Vsw 4#:IL

Vin=48V Vout=12V

Fig8-10 SCP waveform

9 Detailed Descriptions

9.1 Main Control Loop

The PL59201 is a 100V synchronous buck controller with all of the functions necessary to implement a high efficiency step-down power supply. The output voltage range is from 0.8V to 60V. The voltage-mode control architecture uses input feedforward for excellent line transient response over a wide VIN range. Voltage-mode control supports the wide duty cycle range for high input voltage and low dropout applications as well as when a high voltage conversion ratio is required. Current sensing for cycle-by-cycle current limit can be implemented with either the low-side FET RDS(on) or a current sense resistor. The operating frequency is programmable from 100 kHz to 1 MHz. The PL59201 drives external high-side and low-side NMOS power switches with robust 7.5V gate drivers suitable for standard threshold MOSFETs. Adaptive dead-time control between the high-side and low-side drivers minimizes body diode conduction during switching transitions. An external bias supply can be connected to the VCC pin to improve efficiency in high-voltage applications.

9.2 Functional Block Diagram

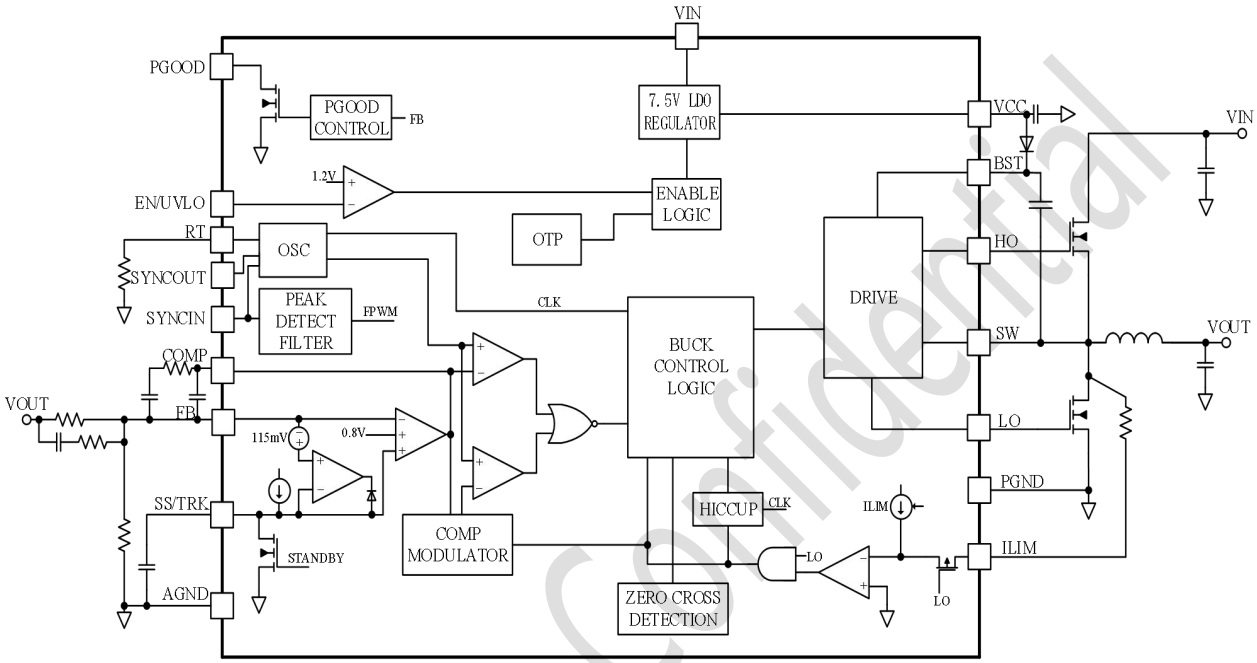


Fig9.2 Block Diagram

9.3 Precision Enable (EN/UVLO)

The EN/UVLO input supports adjustable input undervoltage lockout (UVLO) with hysteresis programmed by the resistor values for application specific power-up and power-down requirements. EN/UVLO connects to a comparator-based input referenced to a 1.2V bandgap voltage. An external logic signal can be used to drive the EN/UVLO input to toggle the output ON and OFF and for system sequencing or protection. The simplest way to enable the operation of the PL59201 is to connect EN/UVLO directly to VIN. This allows self start-up of the PL59201 when VCC is within its valid operating range.

9.4 High-Voltage Bias Supply Regulator (VCC)

The PL59201 contains an internal high-voltage VCC regulator that provides a bias supply for the PWM controller and its gate drivers for the external MOSFETs. The input pin (VIN) can be connected directly to an input voltage source up to 100 V. The output of the VCC regulator is set to 7.5V. However, when the input voltage is below the VCC setpoint level, the VCC output tracks VIN with a small voltage drop. Connect a ceramic decoupling capacitor between 1 μF and 5 μF from VCC to AGND for stability.

Internal power dissipation of the VCC regulator can be minimized by connecting the output voltage or an auxiliary bias supply rail (up to 13V) to VCC using a diode DVCC.

9.5 Power Good Monitor (PGOOD)

The PL59201 provides a PGOOD flag pin to indicate when the output voltage is within a regulation window.

PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 13V. The typical range of pullup resistance is 10kΩ to 100kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail.

9.6 Switching Frequency (RT, SYNCIN)

There are two options for setting the switching frequency, FSW, of the PL59201, thus providing a power supply designer with a level of flexibility when choosing external components for various applications. To adjust the frequency, use a resistor from the RT pin to AGND, or synchronize the PL59201 to an external clock signal through the SYNCIN pin.

Adjust the PL59201 free-running switching frequency by using a resistor from the RT pin to AGND. The switching frequency range is from 100 kHz to 1 MHz. The frequency set resistance, RRT, is governed by Equation 1. E96 standard-value resistors for common switching frequencies are given in Fig9.6.1.

$$R_{RT}[k\Omega] = \frac{10^4}{F_{SW}[kHz]} \quad (1)$$

SWITCHING FREQUENCY (kHz)	FREQUENCY SET RESISTANCE (kΩ)
100	100
200	49.9
250	40.2
300	33.2
400	24.9
500	20
750	13.3
1000	10

Fig9.6.1. Frequency Set Resistors

Apply an external clock synchronization signal to the PL59201 to synchronize switching in both frequency and phase. Requirements for the external clock SYNC signal are:

Clock frequency range: 100 kHz to 1 MHz

Clock frequency: –20% to +50% of the free-running frequency set by RRT

Clock maximum voltage amplitude: 13V

Clock minimum pulse width: 50ns

9.7 Configurable Soft Start (SS/TRK)

After the EN/UVLO pin exceeds its rising threshold of 1.2V, the PL59201 begins charging the output to the DC level dictated by the feedback resistor network. The PL59201 features an adjustable soft start (set by a capacitor from the SS/TRK pin to GND) that determines the charging time of the output. A 10-μA current source charges this soft-start capacitor. Soft start limits inrush current as a result of high output capacitance to avoid an overcurrent condition. Stress on the input supply rail is also reduced. The soft-start time, tSS, for the output voltage to ramp to its nominal level is set by Equation 2.

$$t_{SS} = \frac{C_{SS} * V_{REF}}{I_{SS}} \quad (2)$$

where

• C_{SS} is the soft-start capacitance

• V_{REF} is the 0.8V reference

• I_{SS} is the 10μA current sourced from the SS/TRK pin More simply, calculate CSS using Equation 5.

$$C_{SS}(nF) = 12.5 * t_{SS}(ms)$$

The SS/TRK pin is internally clamped to VFB + 115 mV to allow a soft-start recovery from an overload event. The clamp circuit requires a soft-start capacitance greater than 2 nF for stability and has a current limit of approximately 2 mA.

The SS/TRK pin also doubles as a tracking pin when master-slave power-supply tracking is required. This tracking is achieved by simply dividing down the output voltage of the master with a simple resistor network. Coincident, ratiometric, and offset tracking modes are possible.

If an external voltage source is connected to the SS/TRK pin, the external soft-start capability of the PL59201 is effectively

disabled. The regulated output voltage level is reached when the SS/TRACK pin reaches the 0.8V reference voltage level. It is the responsibility of the system designer to determine if an external soft-start capacitor is required to keep the device from entering current limit during a start-up event. Likewise, the system designer must also be aware of how fast the input supply ramps if the tracking feature is enabled.

Two practical tracking configurations, ratiometric and coincident, are shown in Fig9.7.1. The most common application is coincident tracking, used in core versus I/O voltage tracking in DSP and FPGA implementations. Coincident tracking forces the master and slave channels to have the same output voltage ramp rate until the slave output reaches its regulated setpoint. Conversely, ratiometric tracking sets the output voltage of the slave to a fraction of the output voltage of the master during start-up.

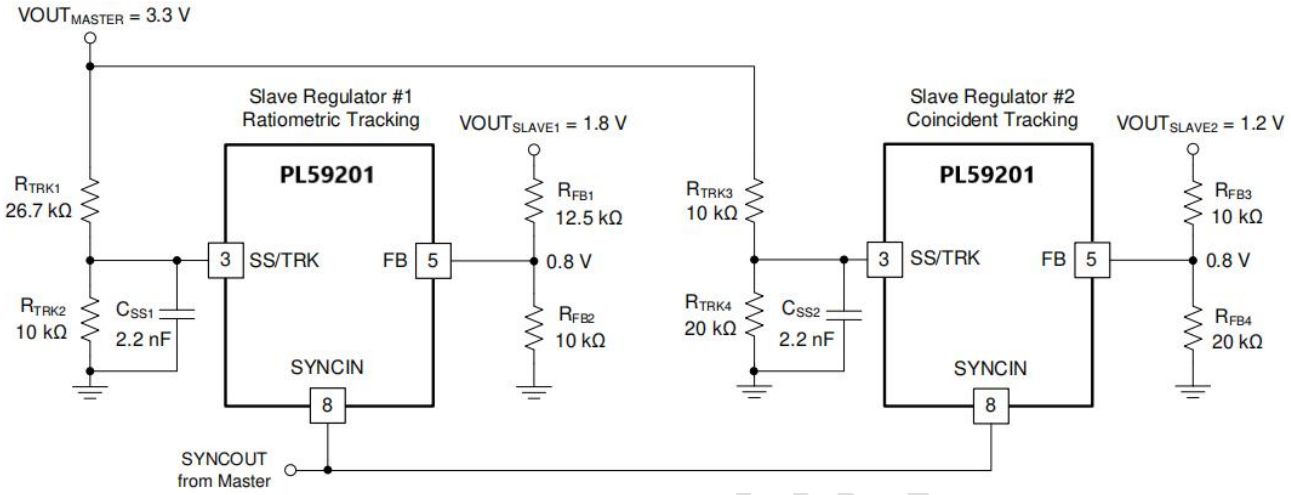


Fig9.7.1 Tracking Implementation With Master, Ratiometric Slave, and Coincident Slave Rails

For coincident tracking, connect the SS/TRK input of the slave regulator to a resistor divider from the output voltage of the master that is the same as the divider used on the FB pin of the slave. In other words, simply select RTRK3 = RFB3 and RTRK4 = RFB4 as shown in Fig9.7.1. As the master voltage rises, the slave voltage rises identically (aside from the 80-mV offset from SS/TRK to FB when VFB is below 0.8 V). Eventually, the slave voltage reaches its regulation voltage, at which point the internal reference takes over the regulation while the SS/TRK input continues to 115 mV above FB, and no longer controls the output voltage.

9.8 Current Sensing and Overcurrent Protection (ILIM)

The PL59201 implements a lossless current sense scheme designed to limit the inductor current during an overload or short-circuit condition. Fig9.8.1 portrays the popular current sense method using the on-state resistance of the low-side MOSFET. Meanwhile, Fig9.8.2 shows an alternative implementation with current shunt resistor, RS. The PL59201 senses the inductor current during the PWM off-time (when LO is high).

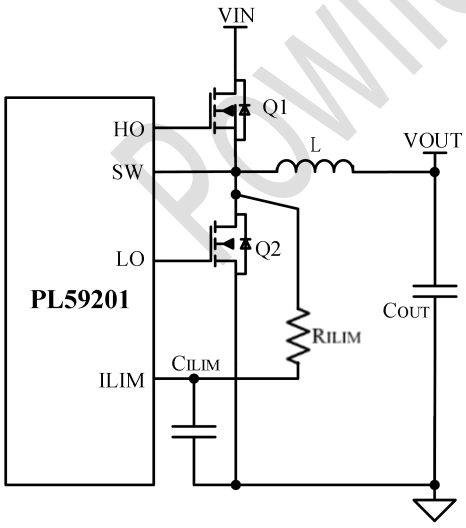


Fig9.8.1 MOSFET RDS(on) Current Sensing

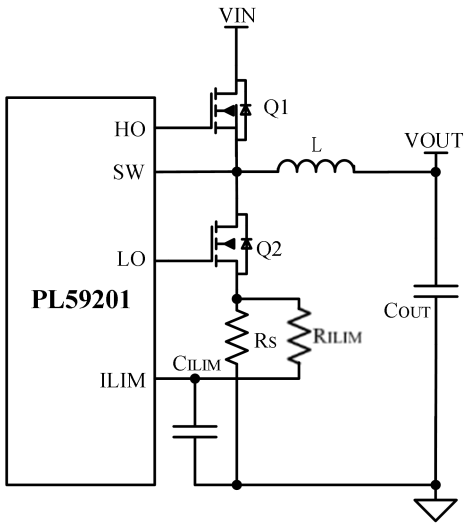


Fig9.8.2 Shunt Resistor Current Sensing

The ILIM pin of the PL59201 sources a reference current that flows in an external resistor, designated RILIM, to program of the current limit threshold. A current limit comparator on the ILIM pin prevents further SW pulses if the ILIM pin voltage goes below GND.

Resistor RILIM is tied to SW to use the RDS(on) of the low-side MOSFET as a sensing element (termed RDS(on) mode). Alternatively, RILIM is tied to a shunt resistor connected at the source of the low-side MOSFET (termed RSENSE mode). The PL59201 detects the appropriate mode at start-up and sets the source current amplitude and temperature coefficient (TC) accordingly.

The ILIM current with RDS-ON sensing is 200 µA at 27°C junction temperature and incorporates a TC of +4500 ppm/°C to generally track the RDS(on) temperature variation of the low-side MOSFET. Conversely, the ILIM current is a constant 100 µA in RSENSE mode. This controls the valley of the inductor current during a steady- state overload at the output. Depending on the chosen mode, select the resistance of RILIM using Equation 3.

$$R_{ILIM} = \begin{cases} \dfrac{I_{OUT} - \Delta I_L/2}{I_{RDSON}} \cdot R_{DS(on)Q2}, & R_{DS(on)} \text{ sensing} \\ \dfrac{I_{OUT} - \Delta I_L/2}{I_{RS}} \cdot R_S, & \text{shunt sensing} \end{cases} \quad (3)$$

Where:

ΔIL is the peak-to-peak inductor ripple current

RDS(on)Q2 is the on-state resistance of the low-side MOSFET

IRDSON is the ILIM pin current in RDS-ON mode

RS is the resistance of the current-sensing shunt element, and IRS is the ILIM pin current in RSENSE mode.

Given the large voltage swings of ILIM in RDS(on) sensing mode, a capacitor designated CILIM connected from ILIM to PGND is essential to the operation of the valley current limit circuit. Choose this capacitance such that the time constant RILIM · CILIM is approximately 6 ns.

Note that current sensing with a shunt component is typically implemented at lower output current levels to provide accurate overcurrent protection. Burdened by the unavoidable efficiency penalty, PCB layout, and additional cost implications, this configuration is not usually implemented in high-current applications (except where OCP setpoint accuracy and stability over the operating temperature range are critical specifications).

9.9 Device Functional Modes

9.9.1 Shutdown Mode

The EN/UVLO pin provides ON / OFF control for the PL59201. When the EN/UVLO voltage is below 0.37V (typical), the device is in shutdown mode. Both the internal bias supply LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 13.5µA (typical) at VIN = 48V . The PL59201 also includes undervoltage protection of the internal bias LDO. If the internal bias supply voltage is below its UVLO threshold level, the switching regulator remains off .

9.9.2 Standby Mode

The internal bias supply LDO has a lower enable threshold than the switching regulator. When the EN/UVLO voltage exceeds 0.42V (typical) and is below the precision enable threshold (1.2V typically), the internal LDO is on and regulating. Switching action and output voltage regulation are disabled in standby mode.

9.9.3 Active Mode

The PL59201 is in active mode when the VCC voltage is above its rising UVLO threshold of 5 V and the EN/ UVLO voltage is above the precision EN threshold of 1.2V. The simplest way to enable the PL59201 is to tie EN UVLO to VIN. This allows self start-up of the PL59201 when the input voltage exceeds the VCC threshold plus the LDO dropout voltage from VIN to VCC.

9.9.4 Diode Emulation Mode

The PL59201 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation, the low-side MOSFET is switched off when reverse current flow is detected by sensing of the SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss at no-load and light-load conditions, the disadvantage being slower light-load transient response.

The diode emulation feature is configured with the SYNCIN pin. To enable diode emulation and thus achieve discontinuous conduction mode (DCM) operation at light loads, connect the SYNCIN pin to AGND or leave SYNCIN floating. If forced PWM (FPWM) continuous conduction mode (CCM) operation is desired, tie SYNCIN to VCC either directly or using a pullup resistor. Note that diode emulation mode is automatically engaged to prevent reverse current flow during a prebias start-up. A gradual change from DCM to CCM operation provides monotonic start-up performance.

9.10 Thermal Shutdown

The PL59201 includes an internal junction temperature monitor. If the temperature exceeds 150°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

Turns off the high-side and low-side MOSFETs.

Pulls SS/TRK and PGOOD low.

Turns off the VCC regulator.

Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 15°C (typical).

This is a non-latching protection, and the device will cycle into and out of thermal shutdown if the fault persist

10 Applications and Implementation

10.1 Setting the Output Voltage

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R1 and R2. A value between 10k and 1M is recommended for both resistors. If R1=100k is chosen, then R2 can be calculated to be:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (4)$$

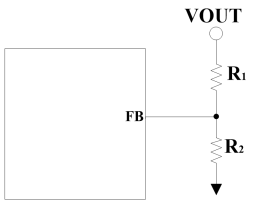


Fig 10.2 Setting Output Voltage

10.2 Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. Why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge and switching losses. Also, at higher frequency the duty cycle of body diode conduction is higher, which results in lower efficiency. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

For a given ripple, the inductance terms in continuous mode are as follows:

$$L = \frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN} - V_{OUT}}{\Delta IL \times F_{SW}} \quad (5)$$

where:

F_{SW} is operating frequency, kHz

L is inductor values,uH

V_{IN} is input voltage, V

V_{OUT} is output voltage, V

ΔIL is maximum inductor ripple current, A, usually select 20~40% maximum output current.

10.3 Power MOSFET Selection

The choice of power MOSFETs has significant impact on DC-DC regulator performance. A MOSFET with low on-state resistance, RDS(on), reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the RDS(on) of a MOSFET, the higher the gate charge and output charge (QG and QOSS respectively), and vice versa. As a result, the product RDS(on) × QG is commonly specified as a MOSFET figure-of-merit. Low thermal resistance ensures that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection in a PL59201 application are as follows:

RDS(on) at VGS = 7.5 V

Drain-source voltage rating, BVDSS, typically 60 V, 80 V or 100 V, depending on maximum input voltage

Gate charge parameters at VGS = 7.5 V

Output charge, QOSS, at the relevant input voltage

Body diode reverse recovery charge, QRR

Gate threshold voltage, VGS(th), derived from the Miller plateau evident in the QG vs. VGS plot in the MOSFET data sheet. With a Miller plateau voltage typically in the range of 2 V to 5 V, the 7.5V gate drive amplitude of the PL59201 provides an adequately-enhanced MOSFET when on and a margin against Cdv/dt shoot-through when off.

10.4 CIN and COUT Selection

Input capacitor CIN is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current, input RMS current is given by:

$$I_{CIN}=I_{OUT(MAX)}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

This input current has a maximum at VIN = 2VOUT, ICIN(MAX) = IOUT(MAX)/2.

The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage.

VOUT ripple is given by:

$$\Delta V_{OUT}\leq\Delta I_L*\left(ESR+\frac{1}{8*f*C_{OUT}}\right) \quad (7)$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

10.5 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during each cycle's turn-on and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1μF to 1μF. CBST should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1μF was selected for this design example.Use an external Schottky diode to charge the bootstrap capacitor, connect the cathode of the diode to the BST pin and anode to VCC.

10.6 PCB Board Layout

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). insert at least one inner plane, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.

1,The PL59201 high-side and low-side gate drivers incorporate short propagation delays, adaptive dead-time control and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times.

2,Place all sensitive analog traces and components such as COMP, FB, RT, ILIM and SS/TRK away from high- voltage switching nodes such as SW, HO, LO or BST to avoid mutual coupling. Use an internal layer or layers as a ground plane or ground planes. Pay particular attention to shielding the feedback (FB) trace from power traces and components.

3.The FB pin's resistive divider must be connected between the (+) terminal of COUT and signal ground. Great care should be taken to route the FB line away from noise sources, such as the inductor or the SW line. Also keep the FB node as small as possible to avoid noise pickup.

4.Connect the ILIM setting resistor from the drain of the low-side MOSFET to ILIM and make the connections as close as possible to the PL59201. The trace from the ILIM pin to the resistor must avoid coupling to a high- voltage switching net.

5.Minimize the loop area from the VCC and VIN pins through their respective decoupling capacitors to the GND pin. Locate these capacitors as close as possible to the PL59201.

11 Application Examples

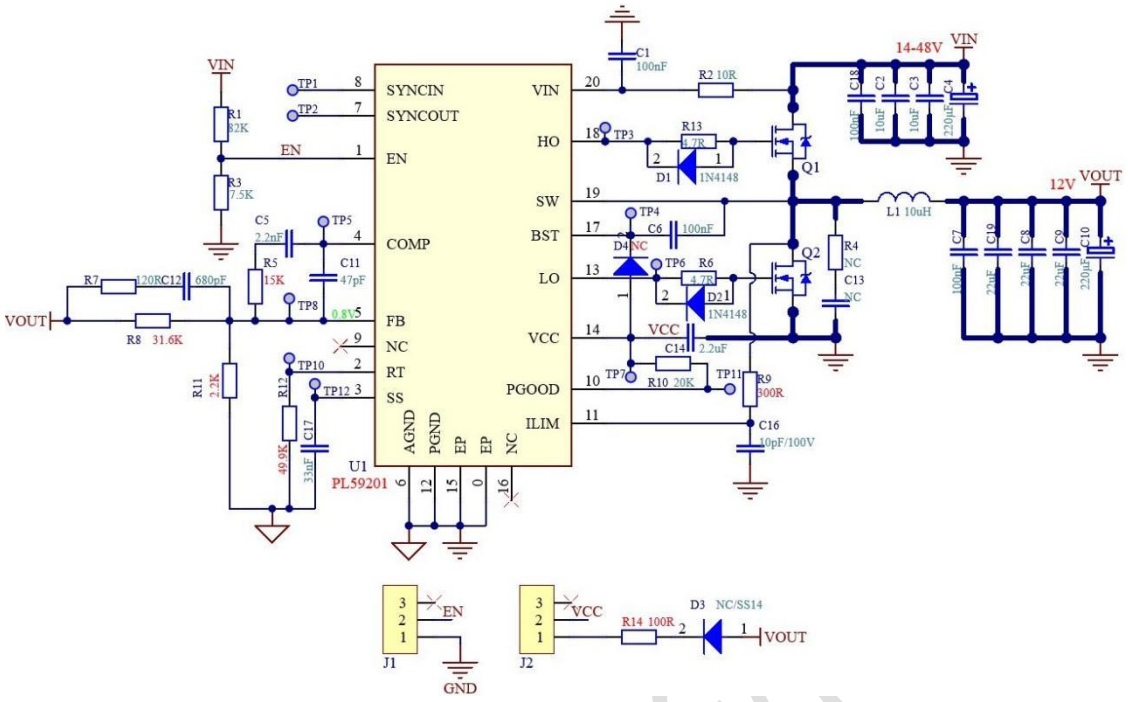


Fig11-1 Schematic

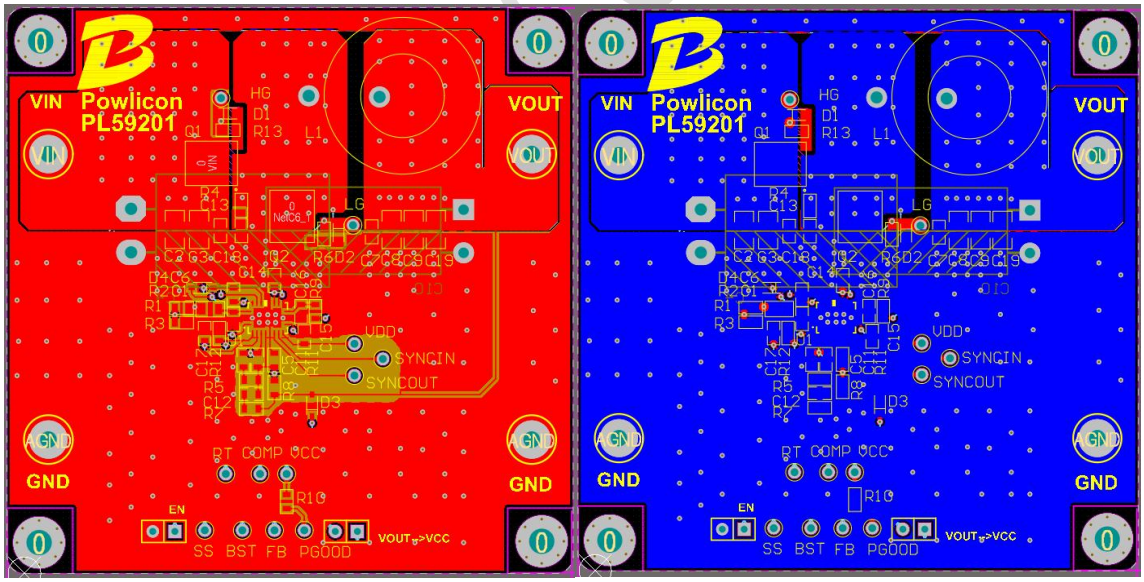
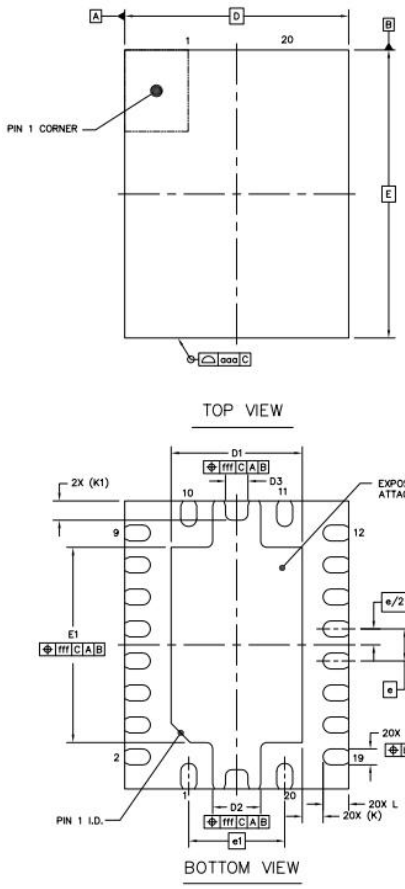


Fig11-2 PCB

12 Packaging Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3.5 BSC	
	Y	E		4.5 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD PITCH		e1		1.5 BSC	
EP SIZE	X	D1	1.95	2.05	2.15
	Y	E1	2.95	3.05	3.15
	X	D2	0.65	0.75	0.85
EP EDGE TO EP EDGE		D3	0.25	0.35	0.45
LEAD LENGTH		L	0.3	0.4	0.5
EP EDGE TO PACKAGE EDGE		K1	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K		0.325 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP · Sn8~20s