32V,Synchronous,High-Efficiency,Boost PWM Controller with Programmable Output Current Limit

1 Features

- 2.8V to 32V Supply Voltage Range
- Integrated 2-A MOSFET Gate Drivers
- External Soft Start (SS)
- Pulse-Skip Mode under Light Loads
- Dynamical programming of Output current and voltage using PWM signal or analog signal
- Adjustable Switching Frequency using resistor
- Frequency dithering for good EMI performance
- Cycle-by-Cycle Peak Current Limit
- Output Average Current Limiting with stable CC loop
- Over-Voltage Protection (OVP)
- Over-Temperature Protection (OTP)
- Support NTC function
- QFN4x4-32 Package

2 Applications

- Backup Boosts
- Start-stop Boosts
- Bluetooth Speakers
- USB Power Delivery

3 Description

The PL5700 adopts constant-on-time (COT) control topology, which provides fast transient response. The 2A gate driver minimizes the power loss of the external MOSFET while allowing the use of a wide variety of standard threshold devices. Additionally, the PL5700 uses pulse-skip mode to improve the efficiency under light loads or no load.

The switching frequency could be set to 150kHz, 300kHz based on different resistor value between FREQ pin and GND pin.

The device also features a programmable soft-start function and VADJ, IADJ pins are used to program output VBUS voltage and output current limit.Under-voltage lockout (UVLO), soft start (SS), an internal regulated supply, and slope compensation are all provided to minimize the external component count.

PL5700 provides voltage control loop, constant current loop. Protection features include hiccup mode for overload protection (OLP), over voltage protection (OVP).

4 Typical Application Schematic

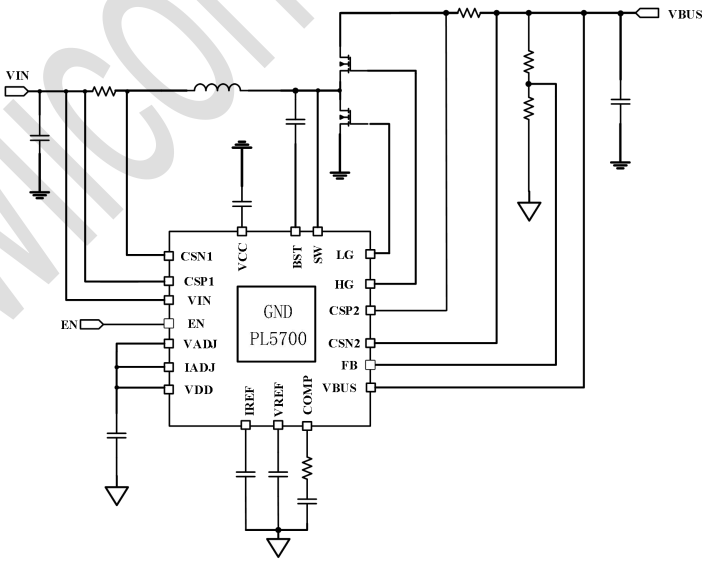


Fig. 1 Application Schematic

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5 Pin Configuration and Functions

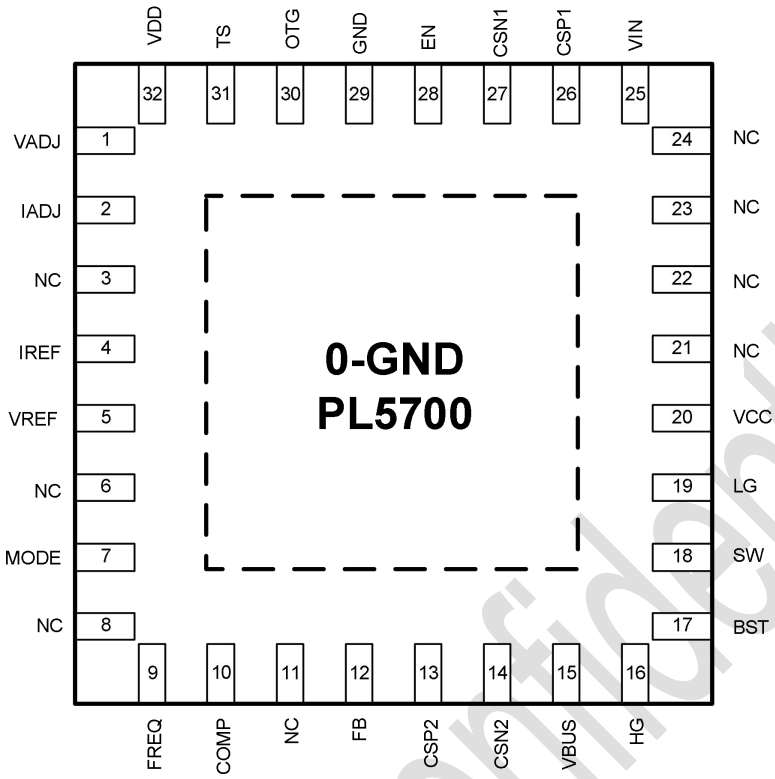


Fig. 2 Pin-Function (QFN4X4-32)

Pin		Description
Number	Name	
1	VADJ	Connect a 0-2V analog voltage or a PWM signal to program voltage reference on VREF pin. Connect this pin to VDD will force VREF to constant 2V.
2	IADJ	Connect a 0-2V analog voltage or a PWM signal to program voltage reference on IREF pin. Connect this pin to VDD will force IREF to 2V.
4	IREF	Reference voltage for input and output current limiting loop.
5	VREF	Voltage reference for voltage control loop.
7	MODE	No actual functionality,Just provide a pull-up for the OTG pin.
9	FREQ	Connect to GND to set the switching frequency at 150kHz. Connect this pin to VDD to set switching frequency at 300kHz.It is recommended to use 150 KHZ.
10	COMP	Error Amplifier output.
12	FB	VBUS voltage feedback. Connect a resistor divider between VBUS and GND to FB to program VBUS voltage in battery discharging mode.
13	CSP2	The positive input of output current sense.
14	CSN2	The minus input of output current sense.
15	VBUS	VBUS voltage.
16	HG	High side MOSFET driver output.
17	BST	Boost pin for high side MOSFET driver.
18	SW	Connect this pin to the Switching point2 of the power stage.
19	LG	Low side MOSFET driver output2.
20	VCC	5.0V power supply for high side and low side driver
25	VIN	Input voltage.
26	CSP1	The minus input current sense.
27	CSN1	The positive input current sense.
28	EN	Logic High will enable the converter. Logic Low will disable the whole PL5700 . EN is pulled high internally by a high value resistor.
3/6/8/11/ 21/22/23/ 24	NC	Must leave them floating.

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29/0	GND	Connect to GND.
30	OTG	Just connect OTG to MODE PIN.
31	TS	Connect to VDD pin.
32	VDD	5.4V power supply for PL5700control core.

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6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL5700	PL5700IQN32	QFN4x4-32	4000	5700 RAAYMD

PL5700: Part Number
RAAYMD: RAA: LOT NO.; YMD: Package Date Code

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7 Specifications

7.1 Absolute Maximum Ratings(Note1)

PARAMETER	MIN	MAX	Unit
VIN, VBUS, CSP1, CSN1, CSP2, CSN2, SW	-0.3	40	V
BST to SW	-0.3	7	
VCC to GND	-0.3	7	
CSP1 to CSN1,CSP2 to CSN2	-0.3	0.6	
VBAT to CSP1, CSN1	-0.3	0.6	
VBUS to CSP2, CSN2	-0.3	0.6	
Other Pins to GND	-0.3	6	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+150	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model		2	kV

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	VIN，VBUS	2.8	32	V
Temperature	Operating junction temperature range, T_J	-40	+125	°C

7.4 Thermal Information(Note 3)

Symbol	Description	QFN4x4-32	Unit
θ_{JA}	Junction to ambient thermal resistance	44	°C/W
θ_{JC}	Junction to case thermal resistance	9	

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

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7.5 Electrical Characteristics (Typical at VIN = 7.4V, T_J =25°C, unless otherwise noted.)

Supply voltages	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VIN	VIN voltage		2.8		32	V
I_Q	VIN Shutdown Current	EN=0V, VIN=7.4V		150		uA
VBUS	Bus line voltage		2.8		32	V
V_{VCC}	Driver power supply voltage	VIN =7.4V		5.0		V
V_{VDD}	Control core power supply voltage	VIN =7.4V		5.4		V
UVLO/EN						
$VIN_{_UV}$	VIN UVLO Rising			2.7		V
	UVLO Hysteresis			200		mV
V_{EN_UV}	Operation Threshold		1.1	1.2	1.3	V
	Hysteresis			200		mV
VREF						
V_{VREF}	VREF voltage	VADJ connected to VDD		2		V
Control loop						
V_{FB}	V_{FB} regulation voltage	FB voltage		2		V
G_{mEA}	Error amplifier gm			450		uS
I_{SINK}	COMP sink/source current	VFB=VREF+100mV		15		uA
I_{SOURCE}	COMP source current	VFB=VREF-100mV		20		uA
I_{FB}	FB bias current	FB in regulation			100	nA
Frequency						
F_{SW}	Switching Frequency	FREQ 0-0.4V, short FREQ pin to GND.		150		KHz
		FREQ 1.8-5.4V, short FREQ pin to VDD.		300		KHz
Current Limit						
I_{CCLIM_BUS}	Bus average current Limit, V_{CSP2} - V_{CSN2}			40		mV
I_{CCLIM_VIN}	Inductor peak current Limit, V_{CSP1} - V_{CSN1}			40		mV
NMOS Driver						
I_{HDRV} (Note 4)	Driver peak source current	VBST-VSW=5.0V		2		A
	Driver peak sink current	VBST-VSW=5.0V		2		A
I_{LDRV} (Note 4)	Driver peak source current	VCC=5.0V		2		A
	Driver peak sink current	VCC=5.0V		2		A
V_{BSTUV}	UVLO			2		V
	UVLO Hysteresis			300		mV
Output Protection						
V_{OVP}	Output over voltage threshold			110		%
V_{UVP}	Output under voltage threshold			50		%
VADJ, IADJ						
V_{TH_VADJ}(Note 4)	VPWM low voltage				0.4	V
	VPWM high voltage		2.5			V
V_{TH_IADJ}(Note 4)	IPWM low voltage				0.4	V
	IPWM high voltage		2.5			V
T_{SD}(Note 4)	Thermal Shutdown Threshold			150		°C
T_{HYS}(Note 4)	Thermal Shutdown Hysteresis			20		°C

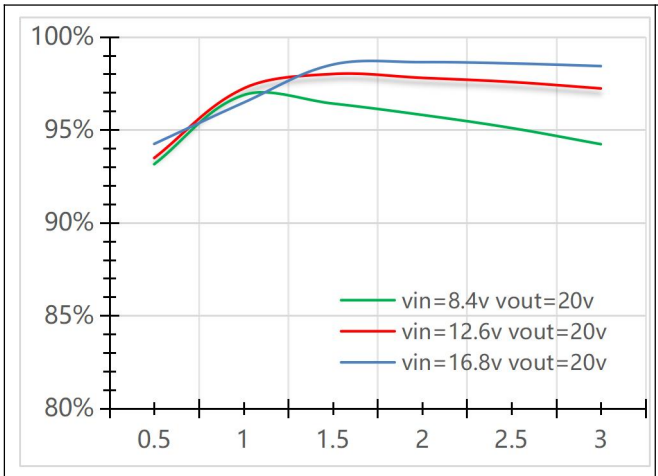
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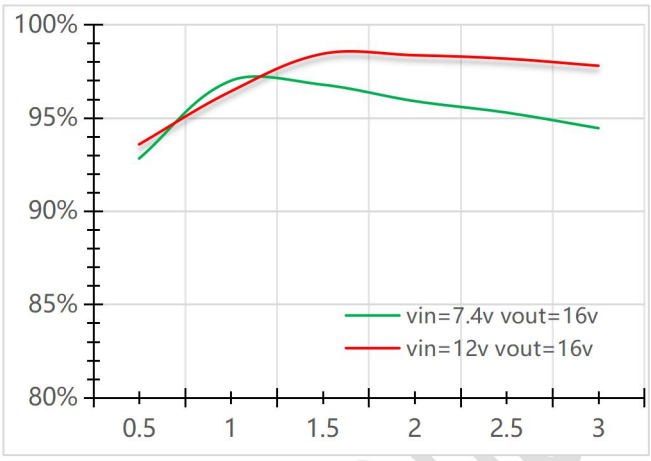
4) Guaranteed by design.

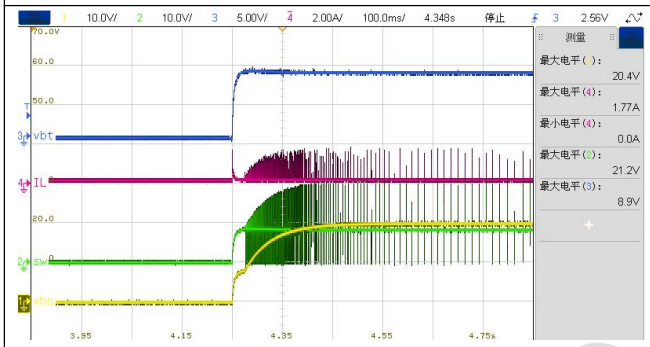
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8 Typical Characteristics

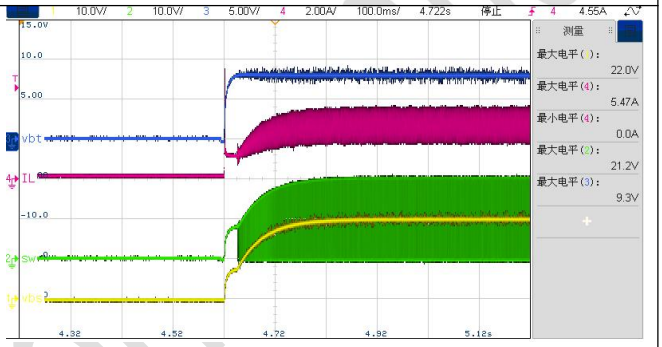






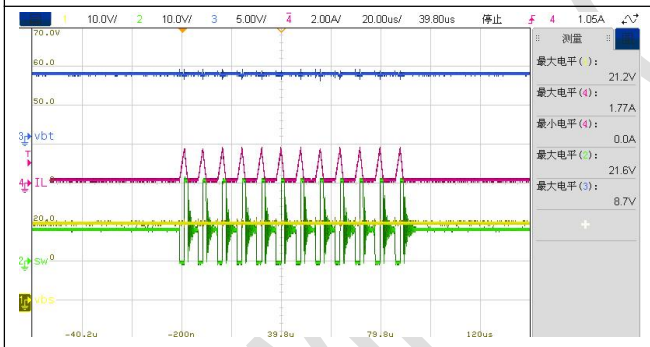
CH1: VOUT CH2:SW CH3:VIN CH4:IL

Vin=8.4V/Vout=20V Start up waveform through Vin, Iout =0A



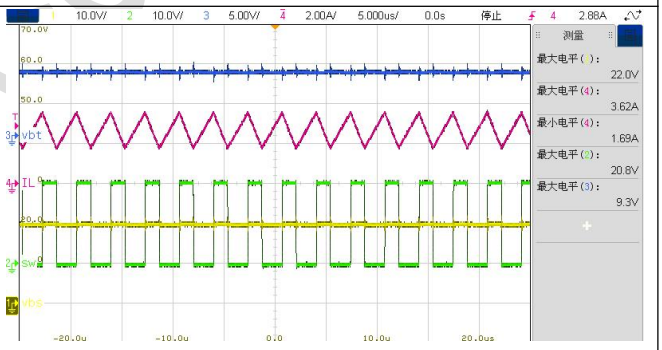
CH1: VOUT CH2:SW CH3:VIN CH4:IL

Vin=8.4V/Vout=20V Start up waveform through Vin, Iout =1A



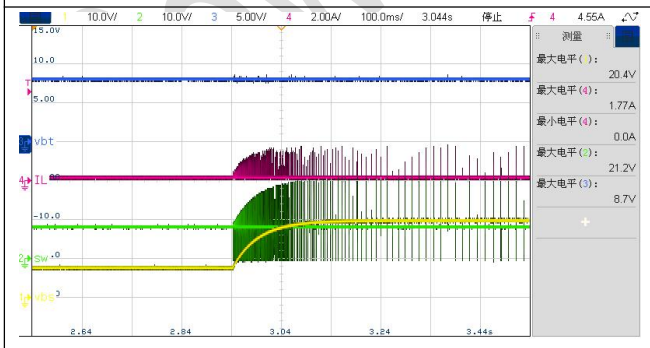
CH1: VOUT CH2:SW CH3:VIN CH4:IL

Vin=8.4V/Vout=20V/Iout =0A Steady state



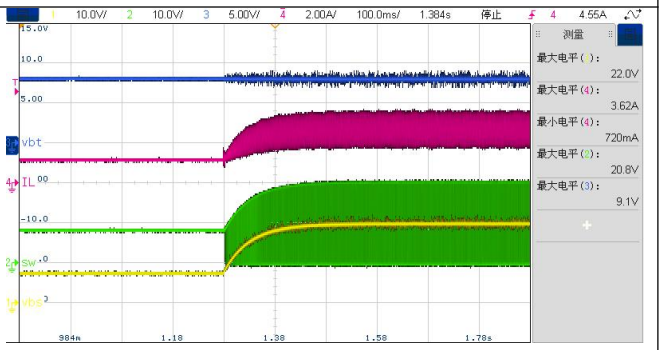
CH1: VOUT CH2:SW CH3:VIN CH4:IL

Vin=8.4V/Vout=20V/Iout =1A Steady state



CH1: VOUT CH2:SW CH3:VIN CH4:IL

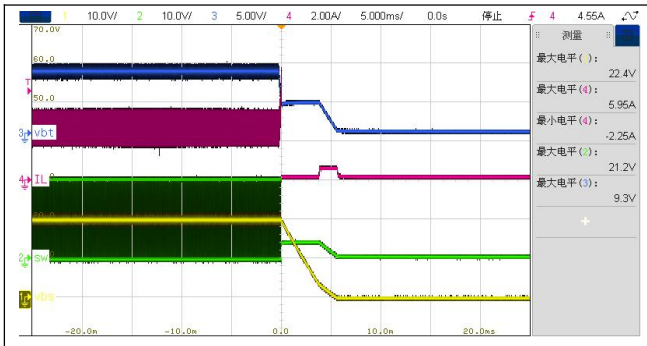
Vin=8.4V/Vout=20V Start up waveform through EN, Iout =0A



CH1: VOUT CH2:SW CH3:VIN CH4:IL

Vin=8.4V/Vout=20V Start up waveform through EN, Iout =1A

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CH1: VOUT CH2:SW CH3:VIN CH4:IL

Vin=8.4V/Vout=20V Shut Down waveform through VIN, Iout =1A



CH1: VOUT CH2:SW CH3:VIN CH4:IL

Vin=8.4V/Vout=20V Shut Down waveform through EN, Iout =1A

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9 Detailed Descriptions

9.1 Overview

The PL5700 is a Constant ON time control mode, PWM boost controller that can drive an external MOSFET capable of handling more than 10A of current , the integrated gate drivers peak current up to 2A.The switching frequency could be set to 150kHz, 300kHz based on different resistor value between FREQ pin and GND pin.

9.2 Enable/UVLO

When EN is greater than 1.2V operating threshold, the control loop starts to work and regulate output to target voltage. When EN pin is below the standby threshold (1.1V typical), PL5700 stops working . EN is pulled high to 4V internally using a 2Meg resistor.

9.3 Over current Protection and short circuit protection

PL5700 provides cycle-by-cycle peak current limit to protect against over current and short circuit conditions. When VOUT is drop to UV threshold, PL5700 will go into hiccup mode to lower down power consumption.If the short circuit condition is removed, the output voltage recovers after the new restart cycle begins.

For boost converters, there is no way to limit the current from the input to the output if the output experiences a short-circuit condition. Use a secondary protection circuit to protect the devices from these conditions.

9.4 Average Output Current Limiting

PL5700 provides optional average current limiting capability to limit the output current. The average current limiting circuit uses an additional current sense resistor connected in series with output voltage of the converter. A current sense gm amplifier with inputs at the CSP2 and CSN2 pins monitors the voltage across the sensing resistor and compares it with an internal 40 mV reference. If the drop across the sense resistor is greater than 40 mV, the gm amplifier regulates COMP voltage to lower down input or output current. The target constant current is given by Equation 1:

$$I_{CL(AVG)} = \frac{40\,mV}{R_{SNS}} \quad (1)$$

9.5 Frequency Setting (FREQ) and frequency dithering

PL5700 switching frequency can be programmed at 150 kHz, 300 kHz or 600 kHz and 1200 kHz by voltage at FREQ pin to GND. When FREQ is connected to AGND, the switching frequency is set at 150 kHz. When FREQ is connected to VDD, the switching frequency is set at 300 kHz.

9.6 Thermal Shutdown

PL5700 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 160°C (typical). The soft-start capacitor is discharged when thermal shutdown is triggered and the gate drivers are disabled. The converter automatically restarts when the junction temperature drops by the thermal shutdown hysteresis of 15°C below the thermal shutdown threshold.

9.7 VREF and IREF

VREF pin is the final reference voltage used in the voltage regulation loop. When VADJ is connected to VDD, VREF will be 2V. When VADJ is connected to a PWM signal, PWM signal will first be chopped to 2V and filter out using an internal resistor and external capacitor on VREF pin. The capacitor on VREF pin is also acting as soft-start capacitor at power up or in output voltage transition period. It is recommend using a relatively large capacitor such as 470nF for VREF pin and IREF pin.

The same mechanism works for IADJ and IREF pin.

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10 Applications and Implementation

The typical application on the first page is a basic PL5700 application circuit. External component selection is driven by the load requirement, and begins with the selection of RS and the inductor value. Next, the power MOSFETs need to be selected. Finally, C_{IN} and C_{OUT} are selected. This circuit can be configured for operation up to an input voltage of 32V.

10.1 R_{CS} Selection

As shown in schematic diagram output current sense resistor RCS should be placed between the bulk capacitor for VBUS and the decoupling capacitor. A low pass filter formed by RF and CF is recommended to reduce the switching noise and stabilize the current loop. Place CSP/CSN, symmetrically and keep them away switching signals such as BST, SW, VIN, VBUS etc.

10.2 Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The inductor current ripple ΔI_L is typically set to 20% to 40% of the maximum inductor current in the boost region at $V_{IN(MIN)}$.

For a given ripple, the inductance terms in continuous mode are as follows:

$$L> \frac{V_{IN(MIN)}^{2}*(V_{OUT}-V_{IN(MIN)})*1000}{f*\Delta I_L*V_{OUT}^{2}} uH \quad (3)$$

where: f is operating frequency, kHz

$V_{IN(MIN)}$ is minimum input voltage, V

$V_{IN(MAX)}$ is maximum input voltage, V

V_{OUT} is output voltage, V

ΔI_L is maximum inductor ripple current, A, usually select 20~40% maximum output current.

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

10.3 C_{IN} and C_{OUT} Selection

The C_{OUT} must be capable of reducing the output voltage ripple because of the discontinuous output current. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{(Cap)}=\frac{I_{OUT(MAX)}*(V_{OUT}-V_{IN(MIN)})}{C_{OUT}*V_{OUT}*f} V \quad (4)$$

where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{(ESR)}=I_{OUT(MAX,BOOST)}*ESR \quad (5)$$

10.4 Output voltage setting

The PL5700 output voltage is set by an external feedback resistive divider carefully placed across the output capacitor. The 1% resistance accuracy of this resistor divider is preferred. The resultant feedback signal is compared with the internal precision 2V voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 2V * \left(1 + \frac{R_1}{R_2}\right) \quad (6)$$

Where R_1 is the upper resistor and R_2 is the lower resistor in the feedback network.

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11 PCB Layout

11.1 Guideline

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistor R1 and R2, should be kept close to the FB pin. Keep VBUS sensing path away from noisy nodes and preferably through a layer on the other side of shielding layer.
2. The input /output bypass capacitor must be placed as close as possible to the VIN/VBUS pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VIN and VBUS pin to reduce the high frequency injection current.
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. Current sensing pairs (CSP,CSN) need to be placed carefully, Layout the lines symmetrically and keep them away from noisy nodes such as BST, SW etc. Connect these nodes directly to the two terminals of current sensing resistors Rcs to form an accurate Kelvin connection.

11.2 Application Examples

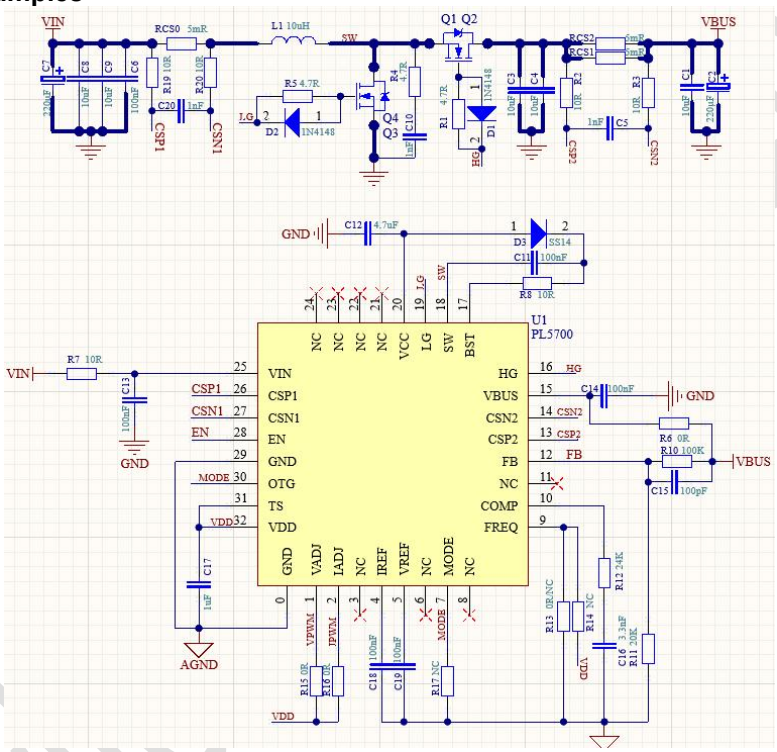


Fig. 3 Application Schematic

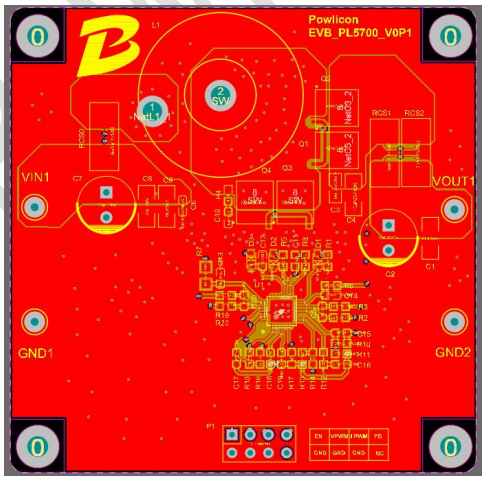


Fig. 32 Top lay

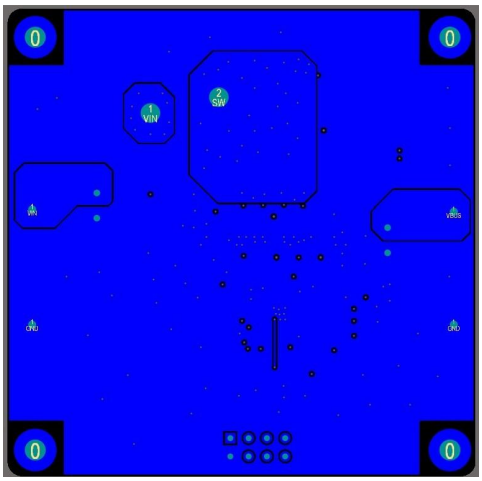
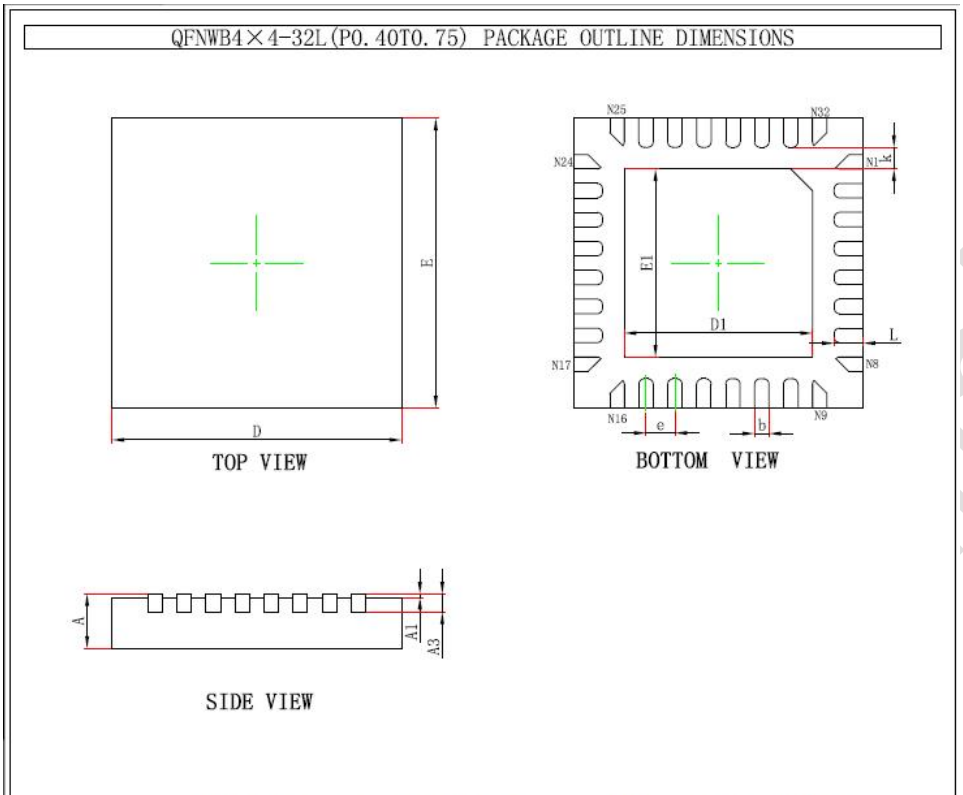


Fig. 33 Bottom

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12 Packaging Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.500	2.700	0.098	0.106
E1	2.500	2.700	0.098	0.106
k	0.300REF.		0.012REF.	
b	0.150	0.250	0.006	0.010
e	0.400BSC.		0.016BSC.	
L	0.300	0.500	0.012	0.020

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