PL62003 High Efficiency, Synchronous bi-directional Buck-Boost Charger with integrated fast charge protocols

1 Features

- Bi-directional buck-boost charging and discharging with PD3.1, QC3.0, AFC, SCP, FCP, BC1.2 protocols integrated
- Support source role, sink role and DRP role for PD3.1
- Charging management, including trickle charging, CC charging, CV charging and charging termination functions
- Wide VBUS and VBAT voltage operation range up to 32V
- Support up to 4 ports (C1 port, C2 port, B port, A port) plug-in and plug-out detection
- Support over current, over voltage protection for each port.
- 1 Cell to 6 Cells battery charge management
- Support both 4.2V and 3.5V battery charging
- Programmable switching frequency 150Khz and 300Khz
- 12-bit DAC converter to guarantee programmable current limit with10mA/step
- 12-bit DAC converter to guarantee programmable output voltage with 5mV/step
- Programmable cable drop compensation
- Integrate N-Gate drivers for up to five USB ports
- Battery voltage, BUS voltage and all ports voltage sensing on VMONP pin
- Battery current, BUS current and all ports current sensing on VMONP pin
- Comprehensive protection features in on-chip buck-boost controller
- Supports pass-through operation when VBUS is close to VBAT
- I^2C interface is available to communicate with MCU
- On-chip LDO to provide power for MCU
- QFN5X5-48 package(**Non-standard**)

2 Applications

- Power Bank
- Battery packs
- Li-ion Battery Charger
- Portable equipments
- General fast Charging
- Smart USB Sockets

3 Description

PL62003 is a high efficiency, synchronous bi-directional buck-boost charger with integrated fast charge protocols. It is a comprehensive and flexible buck-boost charger platform designed for most of fast charging applications with type-C port and PD protocol. It can be programmed to buck charging, boost charging or buck-boost charging. PL62003 provides I^2C interface to communicate with MCU, provides high voltage sensing for battery and BUS terminals, accurate rail-rail current sensing for battery current, BUS current and up-to 4 USB ports currents. It also provides high voltage blocking for CC1, CC2, DP, DM communication signals for all of the USB ports. PL62003 can work with a general MCU to provide a complete, powerful and flexible buck-boost charging system for all kinds of fast charge application such as power bank, battery packs, or portable energy cubic etc.

In charging mode, it steps up or down the input voltage to effectively charge the batteries. PL62003 supports trickle charging, constant current (CC) charging and constant voltage (CV) charging management. The charging current and charging voltage can be programmed by two 12-bit DAC converters.

The PL62003 features I^2C interface, so the user can easily control the charging/discharging mode, and program charging current, charging voltage, output voltage, and output current limits through I^2C. It also monitors the status of up to four USB ports and provides four NMOS gate drivers to control the power path independently. User can also use I^2C to monitor the status of DC-DC, even the whole system.

PL62003 also provides VMONP pin, through which the MCU can monitor VBUS, VBAT voltage, IBUS, IBAT current and the current of each port in real time. All these features simplify the system design and reduce BOM cost for any charging system.

The PL62003 supports under voltage protection, over voltage protection, over current protection, short circuit protection and over temperature protections to ensure system safety under different abnormal conditions.

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4 Typical Application Schematic

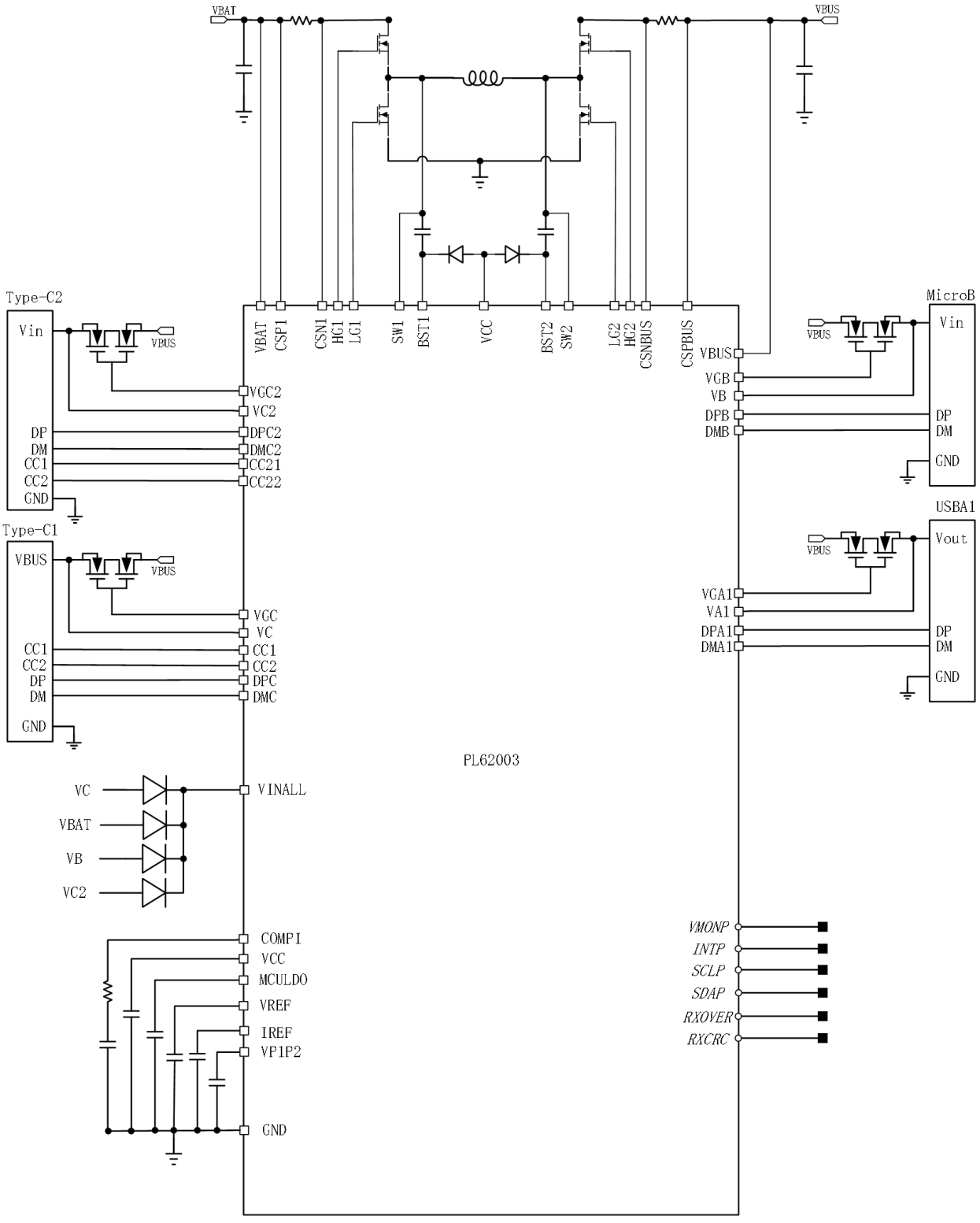


Fig. 4-1 Typical Application Schematic

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5 Pin Configuration and Functions

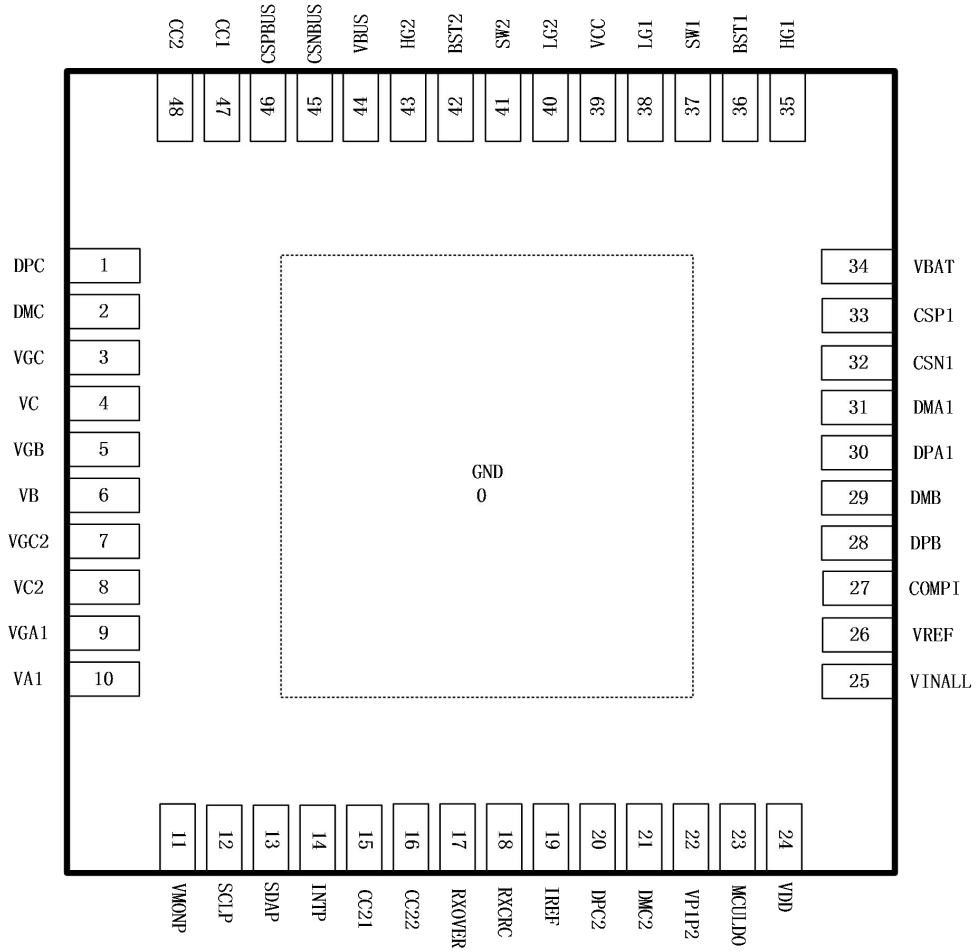


Fig. 5-1 Top view

Tab.5-1 PL62003 Pin-Functions (QFN5X5-48 Package)

Pin		Description
Number	Name	
0	GND	Exposed pad of the package,Ground connection for internal circuits
1	DPC	D+ signal for C1 port
2	DMC	D- signal for C1 port
3	VGC	NMOS gate driver to control the external NMOS of C1 port
4	VC	Used to sense the voltage of C port.
5	VGB	NMOS gate driver to control the external NMOS of B port
6	VB	Used to sense the voltage of B port.
7	VGC2	NMOS gate driver to control the external NMOS of C2 port
8	VC2	Used to sense the voltage of C2 port.
9	VGA1	NMOS gate driver to control the external NMOS of A1 port
10	VA1	Used to sense the voltage of A1 port.
11	VMONP	Used to detect VBUS/VBAT voltage, IBUS/IBAT current, and the voltage drop of cut-off MOS for A/B/C1/C2 ports. Connect this pin to MCU
12	SCLP	I^2C clock line. Connect with a pull up resistor (typical 10kΩ). Connect to MCU

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13	SDAP	I²C data line. Connect with a pull up resistor (typical 10kΩ). Connect to MCU
14	INTP	Open drain output for interrupt signal. Connect to MCU
15	CC21	Configuration Channel 1 for C2 port
16	CC22	Configuration Channel 2 for C2 port
17	RXOVER	Multi-function pin to connect with MCU [00:RXOVER 01: VRDAC2P05 10: CLK1MS 11:IFB_B]
18	RXCRC	Multi-function pin to connect with MCU [00:RXCRC 01: 0.9V 10: CLK_DIGT]
19	IREF	Multi-function pin to connect with MCU [00:IREF 01: FB1 10: ADDSEL 11:IFB_A1]
20	DPC2	D+ signal for C2 port
21	DMC2	D- signal for C2 port
22	VP1P2	1.2V power supply.
23	MCULDO	3.3V voltage output for MCU
24	VDD	Output of internal 5V linear regulator. Connect a 1μF capacitor from VDD pin to GND as close to the IC as possible.
25	VINALL	Power supply to the IC. Connect to power rails with low voltage schottky diodes. Place a 1μF capacitor from this pin to GND as close to the IC as possible.
26	VREF	Reference voltage for voltage control loop
27	COMP	Error amplifier output and input to the PWM comparator. Connect frequency compensation components to this pin.
28	DPB	D+ signal for B port
29	DMB	D- signal for B port
30	DPA1	D+ signal for A1 port
31	DMA1	D- signal for A1 port
32	CSN1	Negative input of a current sense amplifier. Connect to one terminal of the current sense resistor in the VBAT side.
33	CSP1	Positive input of a current sense amplifier. Connect to one terminal of the current sense resistor in the VBAT side.
34	VBAT	Battery voltage or Input voltage. Place a 1μF capacitor from this pin to GND as close to the IC as possible.
35	HG1	High side gate driver of switch MOS
36	BST1	Boot-Strap pin Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver.
37	SW1	Power Switching pin. Connect this pin to the switching node of inductor.
38	LG1	Low side gate driver of switch MOS
39	VCC	Power supply for high side and low side driver
40	LG2	Low side gate driver of switch MOS
41	SW2	Power Switching pin. Connect this pin to the switching node of inductor.
42	BST2	Boot-Strap pin Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver.
43	HG2	High side gate driver of switch MOS
44	VBUS	Power node of the charger.
45	CSNBUS	Negative input of a current sense amplifier. Connect to one terminal of the current sense resistor.
46	CSPBUS	Positive input of a current sense amplifier. Connect to one terminal of the current sense resistor.
47	CC1	Configuration Channel 1 for C1 port
48	CC2	Configuration Channel 2 for C1 port

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6 Device Marking Information

Tab. 6-1 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL62003	PL62003IQN48A	QFN5X5-48	5000	62003 RAAYMD

PL62003: Part Number
RAAYMD: RAA: LOT NO.; YMD: Package Date

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7 Specifications

7.1 Absolute Maximum Ratings (Note1)

Over operating free-air temperature range (unless otherwise noted).

Tab. 7-1-1 Absolute Maximum Ratings

		MIN	MAX	Unit
Voltage range at terminals (Note2)	VC, VBUS, VBAT, VINALL, CSP1, CSN1, CSPBUS, CSNBUS, SW1, SW2	-0.3	40	V
	VA1, VB, VC2	-0.3	30	
	VGA1-VA1, VGB-VB, VGC-VC, VGC2-VC2,	-0.3	15	
	VGA1-VBUS, VGB-VBUS, VGC-VBUS, VGC2-VBUS	-0.3	15	
	BST1 to SW1, BST2 to SW2	-0.3	7	
	HG1 to SW1, HG2 to SW2	-0.3	7	
	CC1, CC2, DPC, DMC	-0.3	22	
	DPB, DMB, DPA1, DMA1	-0.3	15	
	COMPI, VMONP, SCLP, SDAP, INTP, RXOVER, RXCRC, IREF, VP1P2, MCULDO, VDD, VREF, LG1, LG2, CC21, CC22, DPC2, DMC2	-0.3	6.5	
	Others	-0.3	6.5	

7.2 Handling Ratings

Tab. 7-2-1 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+160	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model	2	4	kV
	CDM Charger device model		500	V

7.3 Recommended Operating Conditions (Note 3)

Tab. 7-3-1 Recommended Operating Conditions

		MIN	MAX	Unit
Voltage range at terminals(Note2)	VA, VB, VC, VBUS, VBAT, VPWR, CSP1, CSN1, CSPBUS, CSNBUS, SW1, SW2, VINALL	-0.3	32	V
	VA1, VB, VC2	-0.3	28	
	VGA1-VA1, VGB-VB, VGC-VC, VGC2-VC2,	-0.3	12	
	VGA1-VBUS, VGB- VBUS, VGC- VBUS, VGC2-VBUS	-0.3	12	
	BST1 to SW1, BST2 to SW2	-0.3	6.5	
	HG1 to SW1, HG2 to SW2	-0.3	6.5	
	CC1, CC2, DPC, DMC	-0.3	20	
	DPB, DMB, DPA1, DMA1	-0.3	12	
	COMPI,VMONP, SCLP, SDAP, INTP, RXOVER, RXCRC, IREF, VP1P2, MCULDO, VDD,VREF, LG1, LG2, CC21, CC22, DPC2, DMC2	-0.3	6.5	
	Others	-0.3	6.5	

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7.4 Thermal Information(Note 4)

Tab. 7-4-1 Thermal Information

Symbol	Description	QFN5x5-48	Unit
θ_{JA}	Junction to ambient thermal resistance	43	°C/W
θ_{JC}	Junction to case thermal resistance	8	

Notes:
1) Exceeding these ratings may damage the device.
2) All voltage values are with respect to network ground terminal.
3) The device function is not guaranteed outside of the recommended operating conditions.
4) Measured on approximately 1" square of 1 oz copper.

7.5 Electrical Characteristics

(Typical at VBUS = 12V, VBAT = 3.6V, T_J=25°C, unless otherwise noted.)

Tab. 7-5-1 Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Power supplies						
VBUS	Input voltage on VBUS		3.5		32	V
VBAT	Input voltage on VBAT		3.2		32	V
VINALL	Input voltage on VINALL		3.2		32	V
V_{UVLO_VBUS}	VBUS under-voltage lockout threshold	Charging mode, rising edge		3.5		V
		Hysteresis		180		mV
V_{UVLO_VBAT}	VBAT under-voltage lockout threshold	Discharging mode, Rising edge		3.2	3.3	V
		Hysteresis		220		mV
V_{UVLO_VINALL}	VINALL under-voltage lockout threshold			1.2		V
$I_{Q_shutdown}$	shutdown current	VBAT= 8.4V, EN = 0		0	1	μA
I_{Q_stdby}	Standby current	VBAT= 8.4V, GOACTIVE = 0		60	80	μA
I_{Q_noclk}	Quiescent current with digital CLK disabled	VBAT= 8.4V, GOACTIVE = high, DISCLK = high, ENDCDC=low		2		mA
I_{Q_nodcdc}	Quiescent current with DC-DC disabled	VBAT= 8.4V, GOACTIVE = high, DISCLK = low, ENDCDC=low		12		mA
V_{DD}	VDD regulation voltage	VINALL = 12V, I_{VDD} = 1~70mA	4.9	5.1	5.35	V
I_{VDD_LIM}	VDD regulator current limit	VINALL = 12V, VDD = 4V	40	80	120	mA
V_{MCULDO}	LDO regulation voltage	LDO set to 3.3V, ILDO = 1~50mA	3.23	3.30	3.37	V
V_{VP1P2}	1.2V power supply for BMC voltage	VINALL = 12V, connect 1uF from VP1P2 pin to GND.		1.2		V
V_{VCC}	Power supply for buck-boost drivers	VBAT = 12V, connect 1uF from VCC pin to GND.		6.6		V
Vcp	Charge pump voltage	VBAT = 8.4V, VBUS=0V		7		V
Oscillators						
F_{SW}	Switching frequency	FSW_SET = 00		150		kHz
		FSW_SET = 01		300		kHz
F_{CLK_1ms}	1ms CLK for CC scan and timer			1		kHz
F_{CLK_Dig}	CLK for digital core			8000		kHz
Battery Charging						
V_{BAT_chg}	Battery full-charge voltage	1 cell		4.2		V
		2 cell		2*4.2		V
		3 cell		3*4.2		V

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		4 cell		4*4.2		V
		5 cell		5*4.2		V
		6 cell		6*4.2		V
V_{BAT_chg3p5}	Battery full-charge voltage for 3.5V battery cell	1 cell		3.5		V
		2 cell		2*3.5		V
		3 cell		3*3.5		V
		4 cell		4*3.5		V
		5 cell		5*3.5		V
		6 cell		6*3.5		V
V_{INREG}	VINREG voltage regulation	VREG_SET = 00,	4.4	4.5	4.6	V
		VREG_SET = 01	8	8.1	8.2	V
		VREG_SET = 10	10.7	10.8	10.9	V
		VREG_SET =11	17.9	18	18.1	V
V_{EOC}	End of charge voltage threshold		98%	99%	100 %	
V_{RECHG}	Recharge threshold		96.0 %	97.6%	98.8 %	
V_{CHG_OV}	Battery over charge voltage			105%		
Discharging mode						
V_{VREF}	Reference voltage for voltage loop			2.0		V
V_{IREF}	Reference voltage for current loop			2.0		V
I_{SINK_COMPI}	COMPI sink current	VFB=VREF+100mV		15		uA
I_{SOUR_COMPI}	COMPI source current	VFB=VREF-100mV		20		uA
Port detection						
V_{C1_RDY}	Plug-in detection threshold for port C1 used as charging port		4.3	4.4	4.5	V
V_{B_RDY}	Plug-in detection threshold for port B used as charging port		4.3	4.4	4.5	V
V_{C2_RDY}	Plug-in detection threshold for port C2 used as charging port		4.3	4.4	4.5	V
V_{A1_DET}	Plug-in detection threshold for port A1 used as discharging port		1.9	2	2.1	V
V_{B_DET}	Plug-in detection threshold for port B used as discharging port		1.9	2	2.1	V
I_{COM}	Small current detection threshold for I_{BUS}	Falling edge	10	50	80	mV
PD protocol						
I_{PU_CC13A}	Pull up current for CC1 in 3A mode			330		uA
$I_{PU_CC11p5A}$	Pull up current for CC1 in 1.5A mode			180		uA
I_{PU_CC1USB}	Pull up current for CC1 in default USB mode			80		uA
I_{PU_CC23A}	Pull up current for CC2 in 3A mode			330		uA
$I_{PU_CC21p5A}$	Pull up current for CC2 in 1.5A mode			180		uA
I_{PU_CC2USB}	Pull up current for CC2 in default USB mode			80		uA
R_{d_cc1}	R_d pull down resistor on CC1			5.6		kΩ
R_{d_cc2}	R_d pull down resistor on CC2			5.6		kΩ
Cut-off switch control						
$I_{TURNONC}$	C1 port cut-off switch turn on current			1		uA
$I_{TURNONB}$	B port cut-off switch turn on current			1		uA
$I_{TURNONA1}$	A1 port cut-off switch turn on current			1		uA
$I_{TURNONC2}$	C2 port cut-off switch turn on current			1		uA
I^2C						

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V_{IL}	SCLP, SDAP input low voltage		0.4	V
V_{IH}	SCLP, SDAP input high voltage		1.2	V
THERMAL SHUTDOWN				
T_{SD}	Thermal shutdown temperature	Rising	165	°C
		Hysteresis	15	°C

Note:
1) Guaranteed by design

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8 Typical Characteristics

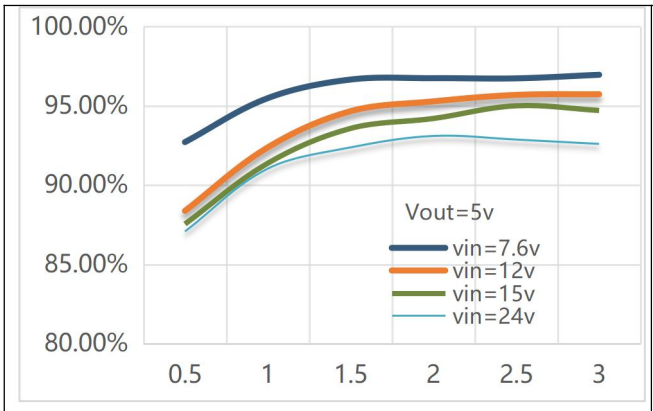


Fig. 8-1 Efficiency

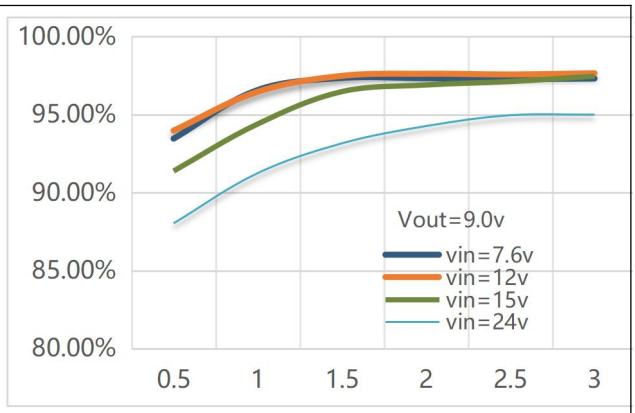


Fig. 8-2 Efficiency

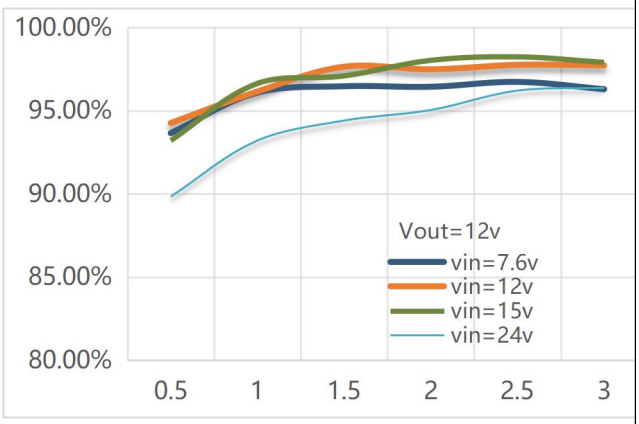


Fig. 8-3 Efficiency

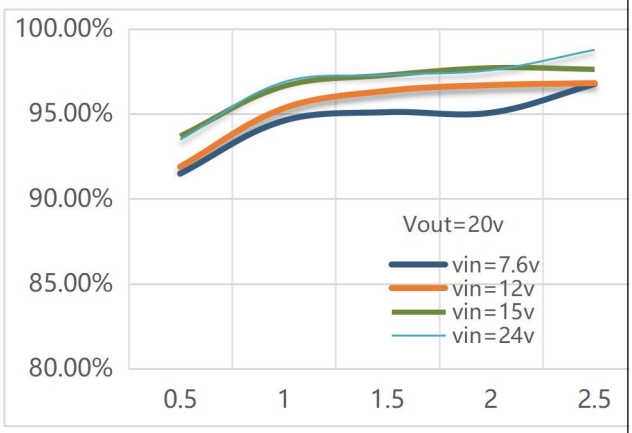
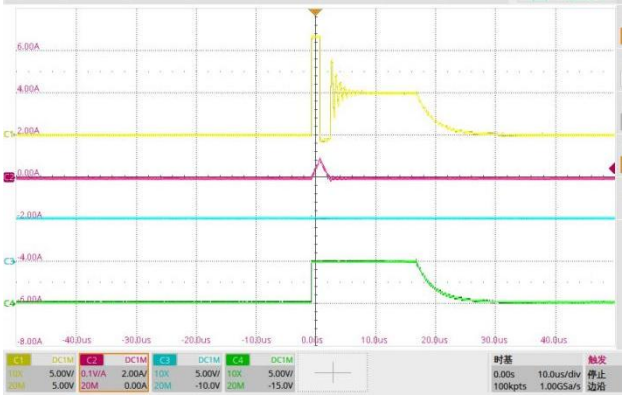


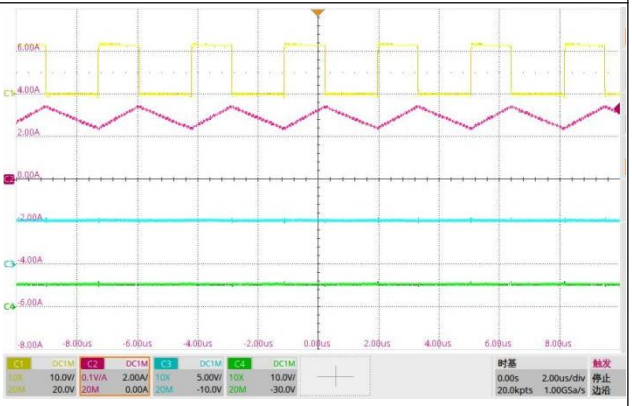
Fig. 8-4 Efficiency



CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=5V

Fig. 8-5 Steady State waveform, Iout=0A

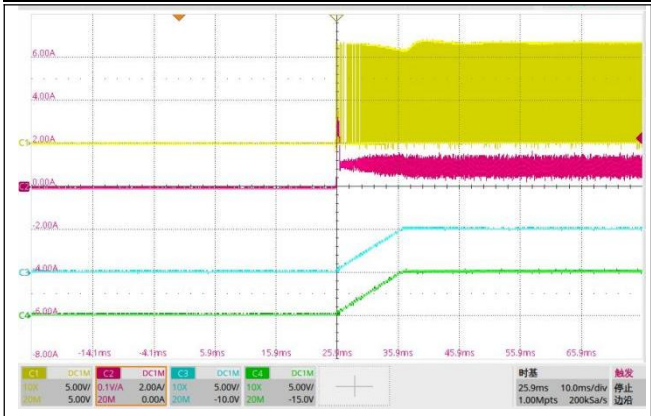


CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=5V

Fig. 8-6 Steady State waveform, Iout=3A

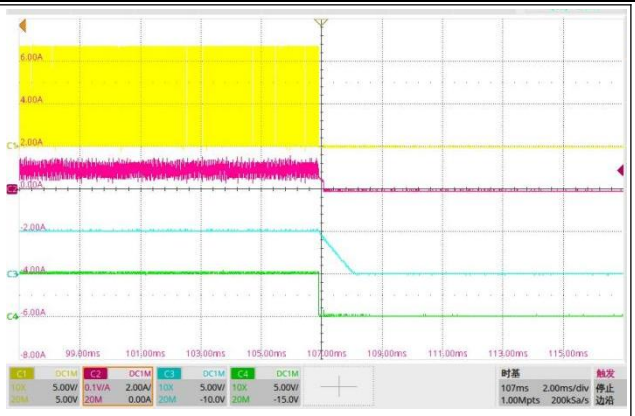
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CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=5V

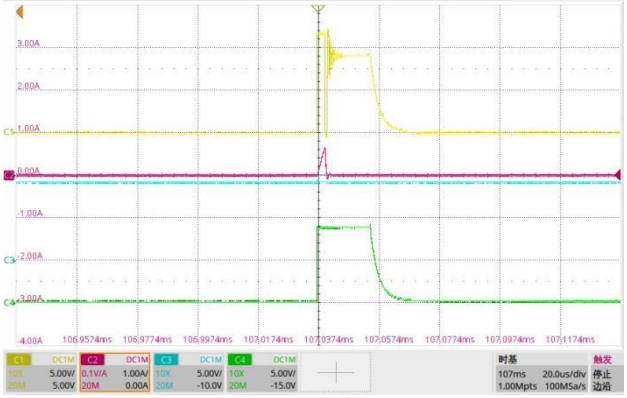
Fig.8-7 Start up waveform, Iout =1A



CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=5V

Fig.8-8 Shut down waveform, Iout =1A



CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=9V

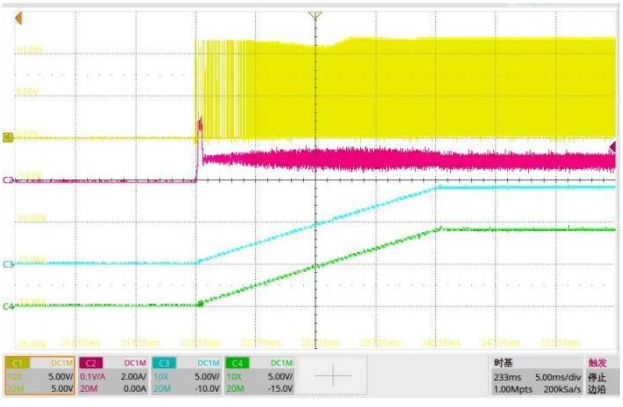
Fig. 8-9 Steady State waveform, Iout=0A



CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=9V

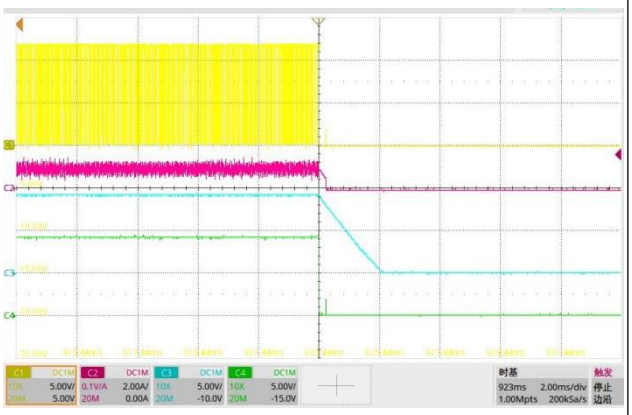
Fig. 8-10 Steady State waveform, Iout=3A



CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=9V

Fig.8-11 Start up waveform, Iout =1A

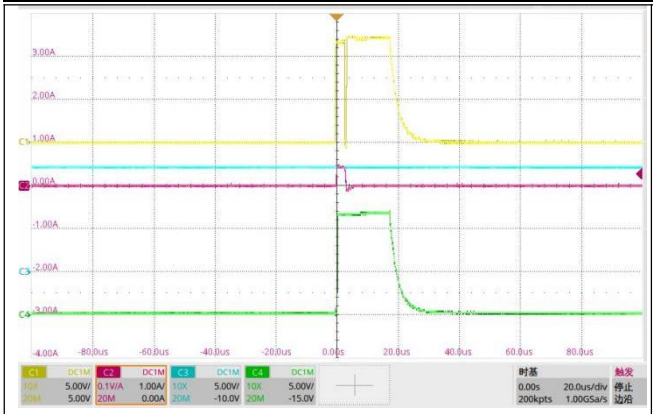


CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=9V

Fig.8-12 Shut down waveform, Iout =1A

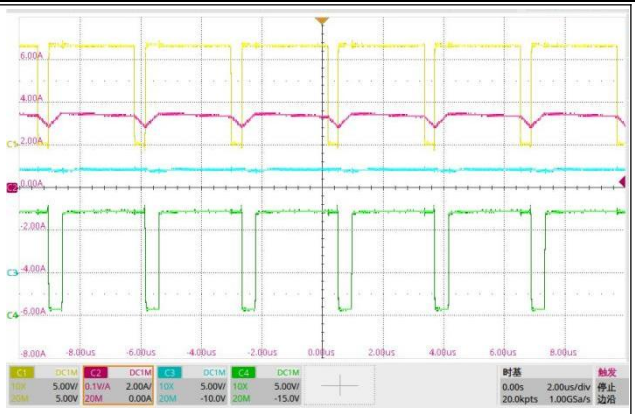
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CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=12V

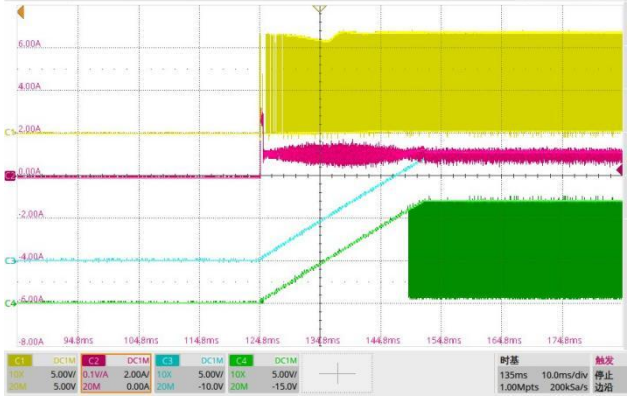
Fig. 8-13 Steady State waveform, Iout=0A



CH1: SW1 CH2:Vout CH3:SW CH4:IL

Vin=12V Vout=12V

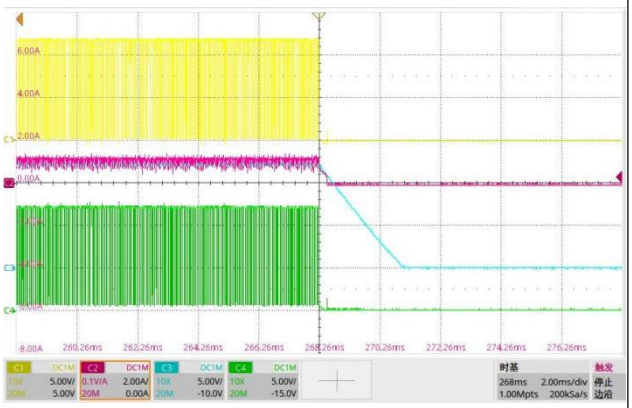
Fig. 8-14 Steady State waveform, Iout=3A



CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=12V

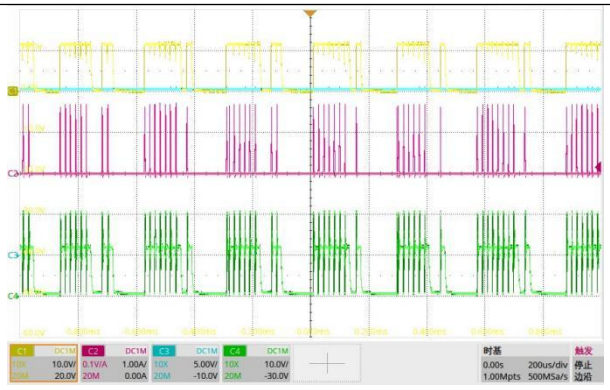
Fig.8-15 Start up waveform, Iout =1A



CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=12V

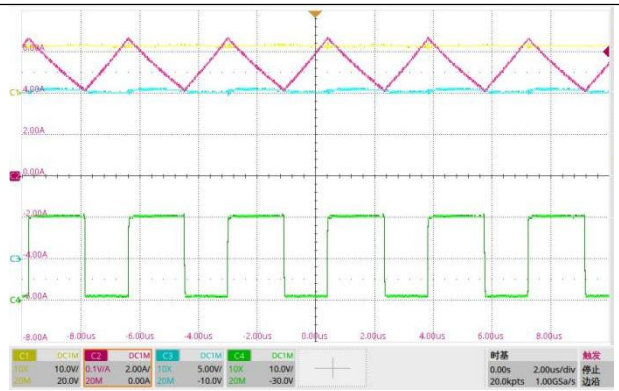
Fig.8-16 Shut down waveform, Iout =1A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=20V

Fig. 8-17 Steady State waveform, Iout=0A

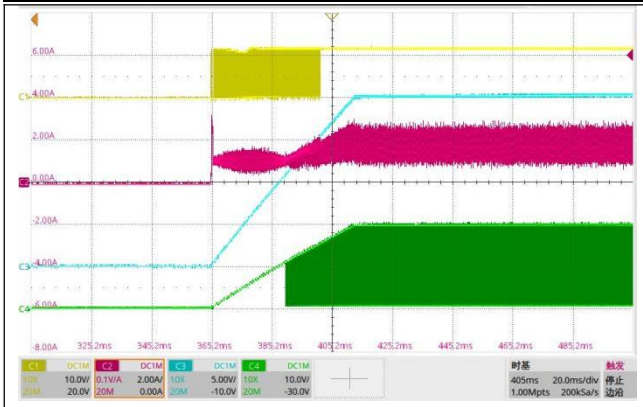


CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=20V

Fig. 8-18 Steady State waveform, Iout=3A

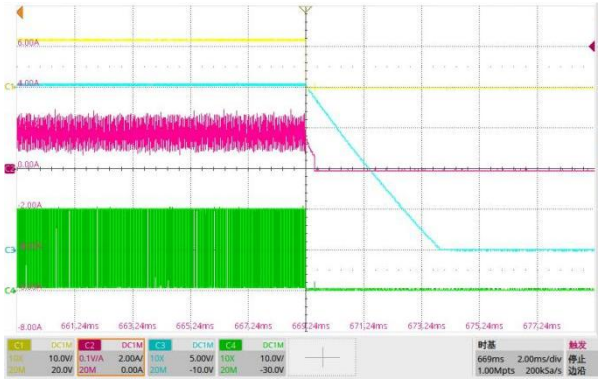
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CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=20V

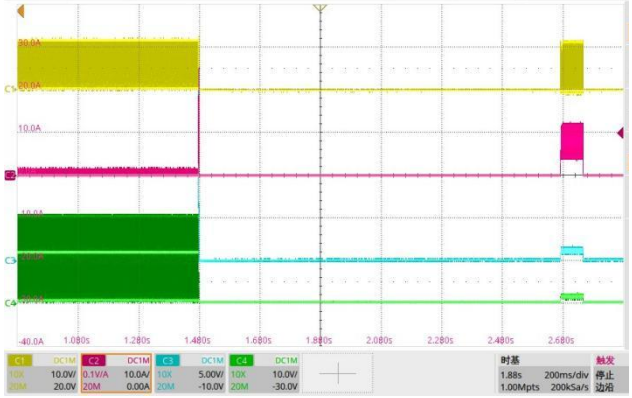
Fig.8-19 Start up waveform, Iout =1A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=20V

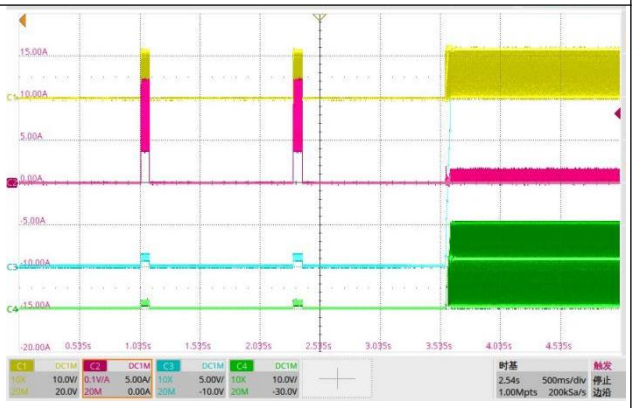
Fig.8-20 Shut down waveform, Iout =1A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=20V

Fig.8-21 Short Circuit waveform



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=20V

Fig.8-22 Short Circuit waveform

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9 Detailed Description

9.1 Overview

PL62003 is a high efficiency, synchronous bi-directional buck-boost charger with integrated fast charge protocols. It is a comprehensive and flexible buck-boost charger platform designed for most of fast charging application with type-C port and PD protocol. It can be programmed to buck charging, boost charging or buck-boost charging. PL62003 provides I²C interface to communicate with MCU, provides high voltage sensing for battery and BUS terminals, accurate rail-rail current sensing for battery current, BUS current and up-to 4 USB ports current. It also provides high voltage blocking for CC1, CC2, DP, DM communication signals for all of the USB ports. PL62003 can work with a general MCU to provide a complete, powerful and flexible buck-boost charging system for all kinds of fast charge application such as power bank, battery packs, or portable energy cubic etc.

9.2 Functional Block Diagram

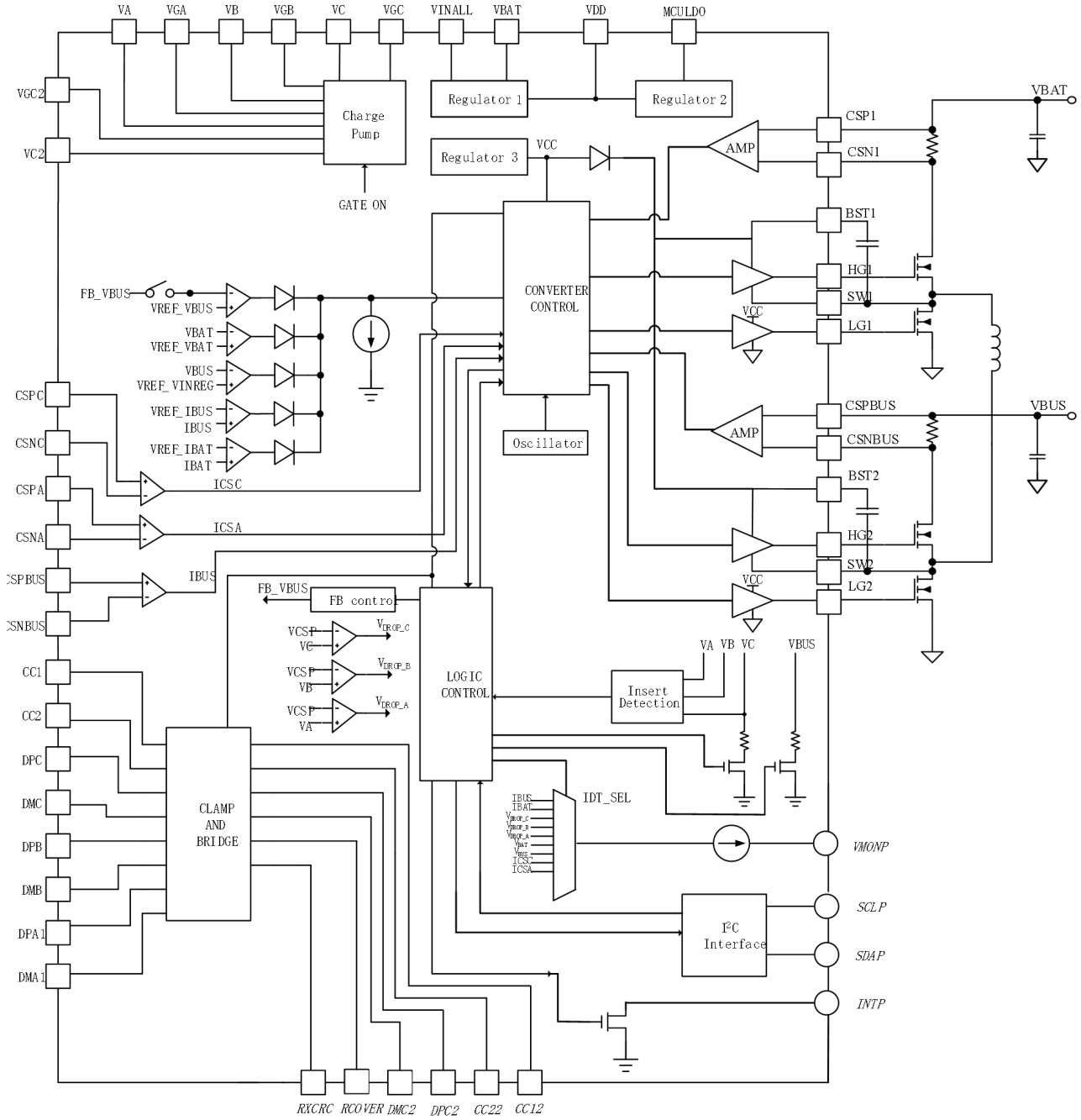


Fig. 9-2-1 PL62003 Diagram

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9.3 Charging Mode

Two registers are used for charge setting: CHG_CTR1 (0X04H) and CHG_CTR2 (0X05H). In order to charge a battery, the following setting are needed to be set up correctly:

1. Use BAT_CELL<2:0> to set up the number of cells in series for battery pack
2. It is optional to use register 0X2EH register to adjust the full battery voltage
3. Set register 0X1BH for a correct adaptive charging VREG point
4. Set bits 0X20H<7:6> to 11 to set IBUS sense gain to 200
5. Set bit 0X2DH<4> high to enable BUS constant current (CC) loop
6. Set correct value for 0X08H register to set up a needed charge current value. When battery voltage is low, set a small value for 0X08H register for trickle charge stage.
7. Set correct value in 0X1CH to turn on the cut-off switch for the corresponding charge port
8. Make sure that the value of battery type bit BATTYPE 0X04H<7> is correct
9. Make sure that OTG bit is 0 for battery charging

After all of the registers are set up correctly, set EN_DCDC bit high to turn on DC-DC and start up to charge battery. During charging, MCU can keep monitoring the status of the whole system by checking status registers and VMONP signal.

The default value of FDCM bit is high, which will force DC-DC to work in forced DCM mode. It is a good choice to start up the system for battery charging in forced DCM mode and set IBUS current limit to a low value. Once the battery voltage ramps above the trickle charge threshold, slowly ramp up IBUS current limit to a higher value (a good choice for IBUS current is 0.5A), then set FDCM bit low to allow the system to work in CCM mode. Sometimes, it may be helpful to make the system transit smoothly from DCM mode to CCM mode by setting VDCMSET<1:0> to 00 to lower down DCM-CCM transition point.

When the battery voltage is very close to full-charge voltage point, it will be better to lower down IREF value slowly by setting 0X08H at lower value. When the inductor current is lower down to be close to be around 0.3A, it is better to set FDCM bit high to force the system working in DCM mode again. When the cell voltage reaches the VBAT target, it enters into Constant Voltage charge phase, and charges the cells with gradually decreased current. Once termination voltage and termination current conditions are satisfied, the IC enters into End of Charge phase if ENEOC bit is high. In this phase the IC will terminate the charging.

User can set ENEOC bit to 0, system will not turn off DC-DC and charge the battery to the setting point. MCU can check battery voltage to determine when to terminate the charge. This mode is especially suitable for small current battery charging such as TWS.

After the battery is fully charged, it is better to disable DC-DC by setting ENDCDC bit low. Sometimes, it may be helpful to set 0X2EH<7> high to force the system go into standby mode to lower down quiescent current to be around 60uA.

If the IC terminates charging after EOC, the battery voltage may drop due to leakage or operation current from battery cells. Once the VBAT voltage drops below VRECH threshold, the IC enters into CC charge phase to recharge the battery. User can also use MCU to monitor battery voltage. Once the battery voltage reaches recharge threshold, MCU can enable the charge again.

During charging, if the IBUS charging current is higher than adapter's current capability, the adapter will be overloaded and VBUS voltage will be pulled lower. PL62003 supports dynamic power management; the allowed minimum VBUS operation voltage for charging is set by VINREG_SET [2:0]. Once VBUS voltage drops to V_{INREG} threshold, the IC reduces the charging current automatically and regulates the VBUS at V_{INREG} threshold. If the VBUS voltage drops below VINREG threshold, the IC reduces the charging current to 0.

9.2 Discharging Mode

When OTG bit is set to1, the IC is set to discharging mode. If FB_SEL is set to 0, internal feedback resistors are used, and the VBUS output is set by 0X06H and 0X07H registers. The default VBUS output voltage is 5V, and can be adjusted from 0V to 20V with 0.5mV per step as below:

$$VBUS\ (V) = 2.15mV \times (VBUS_SET[11] \times 2^{11} + VBUS_SET[10] \times 2^{10} + ...VBUS_SET[0] \times 2^{0})$$

User shall write LDVREF bit to 1 to load the VBUS setting, otherwise the change will not take effect. If constant current loop is needed, user need to set bit 0X2DH<4> high to enable BUS constant current (CC) loop.

9.2.1 PFM Operation

To reduce the switching loss, the IC features Pulse-Frequency Modulation (PFM) operation under light load condition for discharging mode. The IC decreases the frequency automatically to reduce the switching loss so the efficiency can be improved under light load condition. User can also set 0X00H<3> to 1 to force the system to working in CCM mode. FDCM

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bit has higher priority than MODE bit, which means that system will work in DCM mode even if MODE is high with FDCM = 1.

9.2.2 Current Limit in Discharging Mode

When OTG is set to 1, the IC monitors the discharging current through the voltage drop from CSNBUS pin to CSPBUS pin (opposite direction of charging mode). User need to set bit 0X2DH<4> high to enable BUS constant current (CC) loop.

9.3 Port control

PL62003 integrates the port detection and control circuit for up to five USB ports: C1, C2, A and B.

For USB-A port, it can only work as discharging port, and only current from VBUS to VA is allowed. It supports phone insert detection function.

For B port, it can be configured as either charging port or discharging port.

1. If BMODE =1, it works as charging port: adapter insert and removal detection are supported, and the current shall flow from VB to VBUS.
2. If BMODE = 0, it works as discharging port: phone insert detection function is supported, and the current shall flow from VBUS to VB.

For C port, it is normally used for DRP TYPE-C port depending CCMOD<1:0> bits setting in 0X28H register.

9.4 Power Path Management

The IC provides five NMOS gate drivers for A/B/C1/C2 ports respectively.

The NGATE driver must be combined with corresponding port, that is, VGA1 can only be used for VA1 can only be used for VGC1 can only be used for VC1,VGC2 only for VC2, and VGB only for VB .

Either a single NMOS or back-to-back NMOS can be used for each port as shown in typical application circuit. The VGS rating of the NMOS must be considered for the safe operation.

The NGATE driver is controlled by register 0X1CH.

For each port, a full protection system is designed such as over voltage, over current and short-circuits protection.

9.5 Phone Insert Detection

For the discharging port (VA1 or VB with BMODE = 0), phone insert detection function is supported.

While the isolation MOS is off, the port is only biased by an internal weak pull up. After a phone is inserted, the port voltage is pulled low by the operating current of the phone, so the IC can detect the phone attachment. When phone insert is detected, the corresponding interrupt bit (APLOW or BPLOW) is set to inform MCU.

9.6 Adapter Detection

For the charging port (VB with BMODE =1, VC ，VC2), the IC can detect the attachment / detachment of the adapter, and indicate the status through VBRDY, VC1RDY, VC2RDY bits in register 0X36H.

9.7 Small Current Indication

The IC monitors its output port current in discharging mode. Once the port current is lower than 50mA typically, it reports the status to MCU through INT bit.

9.8 Current and Voltage Monitor Function

A specific pin VMONP is used to monitor the system currents and voltages. To turn on VMONP function, set bit 0X1CH<2> high and use register bits 0X2DH<3:0> to select different signals to be sent to VMONP pin. MCU can use ADC to monitor the system status.

9.9 Operation Modes

There are totally 4 operation modes in PL62003: shutdown mode, standby mode, no digital clock mode, no DC-DC mode and normal mode.

1. Shutdown mode: when EN_DCDC bit low, the whole system will be off and I_q will be close to be 0 uA.

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2. Standby mode: if no equipment is attached to PL62003 or 0X2EH<7> is set high, GOACTIVE bit will be low and PL62003 will be in standby mode. I_q will be around 60uA in this mode. Only port detection circuit and MCU LDO are alive in this mode.
3. No digital clock mode: if GOACTIVE is high and DISCLK in register 0X27H is set high, the digital clock will be disabled. All of the power supplies such as VDD, VCC, MCULDO etc. are all alive in this mode. Digital core will be disabled in this mode.
4. No DC-DC mode: if GOACTIVE is high and DISCLK is low, ENDCDC=low, all other circuits are all alive except that DC-DC is disabled.
5. Normal mode: if GOACTIVE is high, DISCLK is low and ENDCDC is high, PL62003 enters normal mode for charging or discharging.

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10 Application and Implementation

10.1 Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The inductor current ripple ΔI_L is typically set to 20% to 40% of the maximum inductor current in the boost region at $V_{IN(MIN)}$.

For a given ripple the inductance terms in continuous mode are as follows:

$$L_{BOOST} > \frac{V_{IN(MIN)}^2 * (V_{OUT} - V_{IN(MIN)}) * 1000}{f * I_{out_max} * 40\% * V_{OUT}^2} \text{ H}$$

$$L_{BUCK} > \frac{V_{OUT} * (V_{IN(MAX)} - V_{OUT}) * 100}{f * \Delta I_L * V_{IN(MAX)}} \text{ H}$$

where: f is operating frequency, kHz

$V_{IN(MIN)}$ is minimum input voltage, V

$V_{IN(MAX)}$ is maximum input voltage, V

V_{OUT} is output voltage, V

ΔI_L is maximum inductor ripple current, A, usually select 20~40% maximum output current.

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

10.2 C_{IN} and C_{OUT} Selection

In boost region, input current is continuous. In buck region, input current is discontinuous. In buck region, the selection of input capacitor C_{IN} is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

$$I_{CIN} = I_{OUT(MAX)} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

This input current has a maximum at $V_{IN} = 2V_{OUT}$, $I_{CIN(MAX)} = I_{OUT(MAX)}/2$.

In the boost region, C_{OUT} must be capable of reducing the output voltage ripple because of the discontinuous output current. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{(BOOST\ ,Cap)} = \frac{I_{OUT(MAX)} * (V_{OUT} - V_{IN(MIN)})}{C_{OUT} * V_{OUT} * f} \text{ V}$$

Where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{(BOOST,ESR)} = I_{OUT(MAX,BOOST)} * ESR$$

In buck mode, V_{OUT} ripple is given by:

$$\Delta V_{OUT} \leq \Delta I_L * \left(ESR + \frac{1}{8 * f * C_{OUT}}\right)$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

10.3 Power MOSFETs Selection and Efficiency Considerations

PL62003 requires four external N-channel power MOSFETs, two for the top switches (switches Q1 and Q4, shown in Figure 1) and two for the bottom switches (switches Q2 and Q3, shown in Figure 1). Important parameters for the power MOSFETs are the breakdown voltage $V_{BR,\ DSS}$, threshold voltage $V_{GS,TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$. The drive voltage is set by the VCC supply.

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In order to select the power MOSFETs, the power dissipated by the device must be known. For switch Q1, the maximum power dissipation happens in the boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{Q1,BOOST}=\left(\frac{V_{OUT}}{V_{IN}}*I_{OUT(MAX)}\right)^2*k*R_{DS(ON)}$$

Where *k* is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature. For a maximum junction temperature of 125°C, using a value *k* = 1.5 to show temperature influence on resistance. $R_{DS(ON)}$ is the normalized value at 25°C.

Switch Q2 operates in the buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{Q2,BUCK}=\frac{V_{IN}-V_{OUT}}{V_{IN}}*I_{OUT(MAX)}^2*k*R_{DS(ON)}$$

Switch Q3 operates in the boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{Q3,BOOST}=\frac{(V_{OUT}-V_{IN})*V_{OUT}}{V_{IN}^2}*I_{OUT(MAX)}^2*k*R_{DS(ON)}+r*V_{OUT}^3*\frac{I_{OUT(MAX)}}{V_{IN}}*C_{RSS}*f$$

Where C_{RSS} is usually specified by the MOSFET manufacturers. The constant *r*, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch Q4, the maximum power dissipation happens in the boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{Q4,BOOST}=\frac{V_{IN}}{V_{OUT}}*\left(\frac{V_{OUT}}{V_{IN}}*I_{OUT(MAX)}\right)^2*k*R_{DS(ON)}$$

For the same output voltage and current, switch Q1 has the highest power dissipation and switch Q2 has the lowest power dissipation unless a short occurs at the output. From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_j=T_a+P*\theta_{TH(JA)}$$

The $\theta_{TH(JA)}$ to be used in the equation normally includes the $\theta_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($\theta_{TH(JC)}$). This value of T_j can then be compared to the original, assumed value used in the iterative calculation process. Based on the T_j requirement for a given MOSFET and regulator efficiency requirement, we can choose suitable part.

10.4 Output voltage setting

PL62003 VBUS voltage is set by an external feedback resistive divider carefully placed across the output capacitor. 1% accuracy resistor is preferred for this divider. The resultant feedback signal is compared with the internal precision VREF voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = VREF * \left(1 + \frac{R_1}{R_2}\right)$$

where R_1 is the upper resistor and R_2 is the lower resistor in the feedback network.

10.5 Current Sense Resistor

A power resistor with 10mΩ or less should be used to sense IBUS current and IBAT current. Resistor of 1% or higher accuracy and low temperature coefficient is recommended.

The resistor power rating and temperature coefficient should be considered. The power dissipation can be roughly calculated as $P=I^2*R$, and I is the RMS current flowing through the resistor. The resistor power rating should be higher than the calculated value.

Normally the resistor value is varied if the temperature increased and the variation is decided by temperature coefficient. If high accuracy of current limit is required, select lower temperature coefficient resistor.

10.6 Isolation MOSFET Selection

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For each port, N-channel MOSFET can be used as isolation switch. When selecting the MOSFET, user shall consider the VGS rating, VDS rating and R_{dson} parameters. When the gate driver is turned on, the IC outputs high voltage based on the lower voltage of VBUS and port voltage. A clamping circuit is designed to guarantee that the VGS voltage will not exceed 8V.

10.7 Diode Selection

PL62003 use VINALL pin to power the internal driver circuits and the LDOs; if a back-to-back isolation is used on a charging port, the port voltage shall also be connected to VINALL pin through a schottky diode. Schottky diodes with small voltage drop such as SS14L are recommended for applications with low battery voltage.

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11 PCB Layout

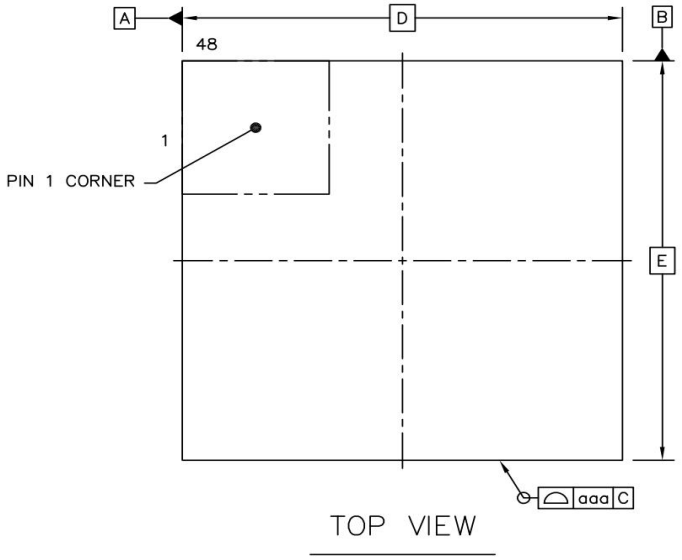
Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The input bypass capacitor must be placed as close as possible to the VBUS pin and ground pin to decouple input noise.
2. The output bypass capacitor must be placed as close as possible to the VBAT pin and ground to decouple output noise.
3. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD.
4. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.
5. CSP1, CSN1, CSPBUS, CSNBUS should directly connected to sensing resistor terminals, and symmetrically route to IC with a kelvin connection style.
6. It is better to separate inductor, power MOSFETs, input bulk capacitor, output bulk capacitor to make a good thermal balance.
7. Put IC away from inductor, power MOSFETs. It is better to use a ground plane

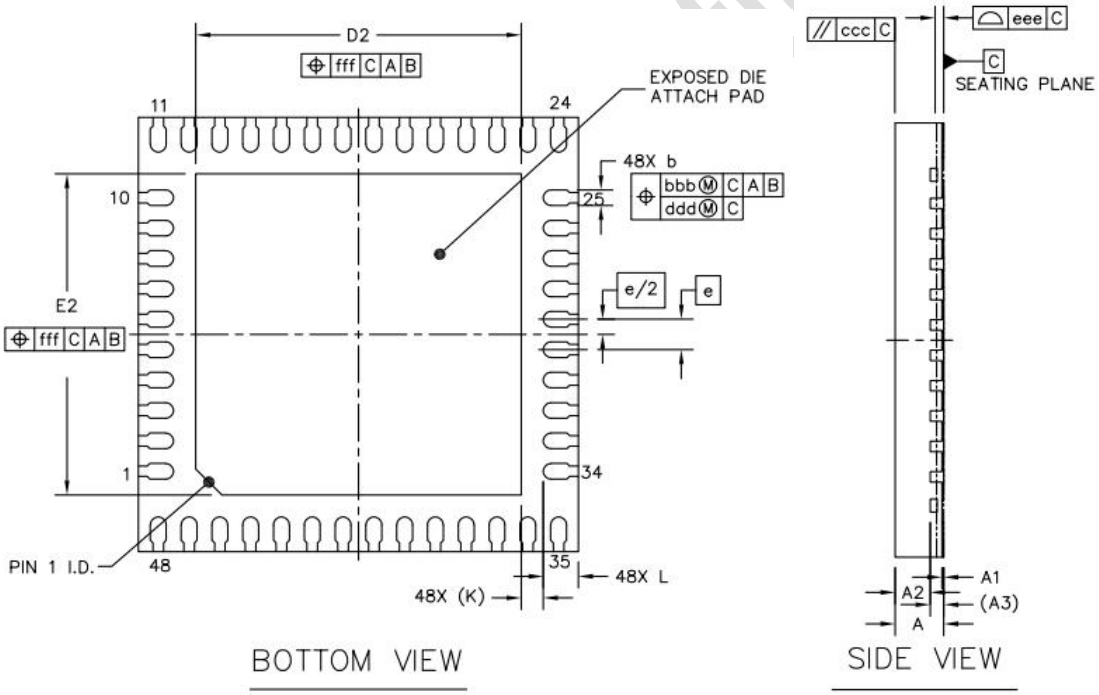
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12 Packaging Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	3.6	3.7	3.8
	Y	E2	3.6	3.7	3.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	



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