17V 6A Synchronous Buck Converter

1 Features

- Integrated 20mΩ/10mΩ MOSFET
- Split Power Rail:2.5V to 20V on PVIN
- 200KHz to 1.6MHz Switching Frequency
- Synchronous to External Clock
- 0.8V±1% Voltage Reference
- Over Temperature Protect
- Low 1uA Shutdown Quiescent Current
- Monotonic Start-Up into Prebiased outputs
- -40°C to 150°C Operating Junction Temperature Range
- Adjustable Slow Start/Power Sequencing
- Power Good Output Monitor for Under voltage & Over voltage
- Adjustable Input Under Voltage Lockout
- QFNFC 3.5*3.5-15L Package

2 Applications

- High Density Distributed Power Systems
- High Performance Point of Load Regulation
- Broadband, Networking and Optical Communication Infrastructure

3 Description

The PL8106 in thermally enhanced 3.5mm*3.5mm QFN package is a full featured 17V,6A synchronous step-down converter which is optimized for small designs through high efficiency and interesting the high-side and low-side MOSFETs. Further space savings are achieved through current mode control, which reduces component, and by selecting a high switching frequency, reducing the inductor's footprint.

The output voltage startup ramp is controlled by the SS/TR pin which allows operation as either a stand alone power supply or in tracking situations. Power sequencing is also possible by correctly configuring the enable and the open drain power good pins.

Cycle by cycle current limit on the high-side feet protects the device in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit which turns off the low-sides MOSFET to prevent excessive reverse current. Thermal shutdown disables the part when die temperature rises too high.

4 Typical Application Schematic

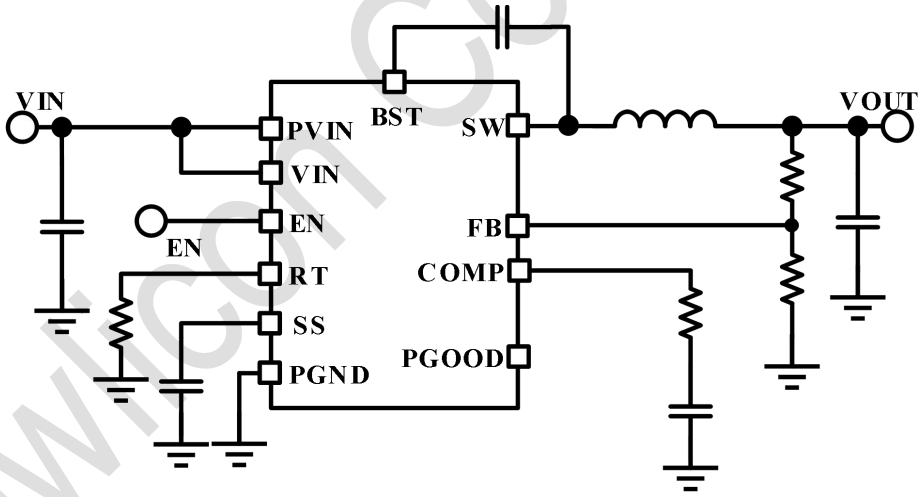


Fig. 4-1 Typical Application Schematic

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5 Pin Configuration and Functions

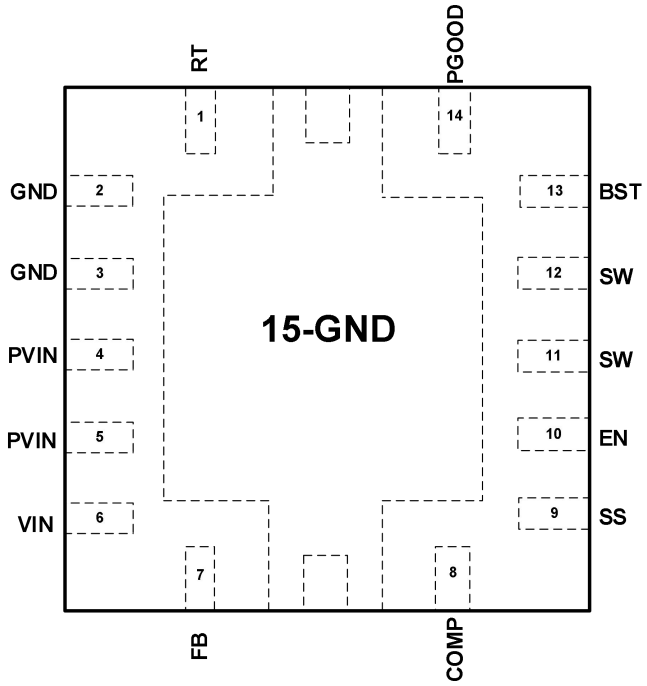


Fig. 5-1 Top view

Tab.5-1 PL8106 Pin-Functions

Pin		Description
Number	Name	
1	RT	Automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device; in CLK mode, the device synchronizes to an external clock.
2,3	GND	Return for control circuitry and low-side power MOSFET.
4,5	PVIN	Power input. Supplies the power switches of the power converter.
6	VIN	Supplies the control circuitry of the power converter.
7	FB	Inverting input of the gm error amplifier.
8	COMP	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
9	SS	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
10	EN	Enable pin. Float to disable. Adjust the input under voltage lockout with two resistors.
11,12	SW	Switch node.
13	BST	A bootstrap cap is required between BOOT and PH. The voltage on this cap carries the gate drive voltage for the high-side MOSFET.
14	PGOOD	Power Good fault pin. Asserts low if output voltage is low because of thermal shutdown, dropout, over voltage, EN shutdown, or during slow start.
15	GND	Thermal pad of the package and signal ground and it must be soldered down for proper operation.

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6 Device Marking Information

Tab. 6-1 Device Marking Information

Order Information	Part Number	Package	Package Qty	Top Marking
PL8106	PL8106IQN15A	QFNFC3.5x3.5 - 15L	4000	8106 RAAYMD

PL8106: Part Number
RAAYMD: RAA: LOT NO.; YMD: Package Date

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7 Specifications

7.1 Absolute Maximum Ratings (Note1)

Over operating free-air temperature range (unless otherwise noted).

Tab. 7-1-1 Absolute Maximum Ratings

	PARAMETER	MIN	MAX	Unit
Voltage range at terminals (Note2)	VIN, PVIN	-0.3	20	V
	BST	-0.3	29	
	SW	-1.0	20	
	BST to SW	0	6	
	RT, PGOOD, EN	-0.3	6	
	FB, COMP, SS	-0.3	3	

7.2 Handling Ratings

Tab. 7-2-1 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+160	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model	2	4	kV
T_A	Operating Ambient Temperature Range	-40	85	°C

7.3 Recommended Operating Conditions (Note 3)

Tab. 7-3-1 Recommended Operating Conditions

	PARAMETER	MIN	MAX	Unit
Input Voltages	VIN	4.5	20	V
Input Voltages	PVIN	2.5	20	V
Output Current		0	6	A
Temperature	Operating junction temperature range, T_J	-40	150	°C

7.4 Thermal Information(Note 4)

Tab. 7-4-1 Thermal Information

Symbol	Description	QFN3.5X3.5-15	Unit
θ_{JA}	Junction to ambient thermal resistance	40.1	°C/W
θ_{JC}	Junction to case thermal resistance	34.4	
θ_{JB}	Junction-to-board thermal resistance	11.4	

Notes:
1) Exceeding these ratings may damage the device.
2) All voltage values are with respect to network ground terminal.
3) The device function is not guaranteed outside of the recommended operating conditions.
4) Measured on approximately 1" square of 1 oz copper.

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7.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 4.5 V to 17 V, PVIN = 2.5 V to 17 V (unless otherwise noted)

Tab. 7-5-1 Electrical Characteristics

Supply voltages	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
PVIN	operating input voltage		2.5		20	V
I_{Q_VIN}	VIN shutdown supply Current	EN=0V		0.1	1	uA
	VIN operating	No Switching, FB=810mV		600	800	uA
VIN	operating input voltage		4.5		20	V
UVLO/EN						
$VIN_{_UV}$	VIN UVLO Rising			4	4.5	V
	UVLO Hysteresis			150		mV
Enable threshold	Rising			1.2	1.26	V
	Falling		0.9	1.0		V
VOLTAGE REFERENCE						
V_{FB}	Voltage reference	0 A ≤ IOUT ≤ 6 A	0.792	0.8	0.808	V
NMOS Driver						
RDSON_HS	HS switch on resistance			20		mΩ
RDSON_LS	LS switch on resistance			10		mΩ
Current Limit						
ILIM_HS	High-side switch current limit threshold		8	13		A
ILIM_LS	Low-side switch sourcing current limit		7	13		A
ILIM_SINK_LS	Low-side switch sinking current limit			2.3		A
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown			150		℃
T_{SD_HYS}	Thermal shutdown hysteresis			15		℃
TIMING RESISTOR AND EXTERNAL CLOCK (RT PIN)						
F_{SW}	Minimum switching frequency	Rrt = 240 kΩ (1%)	160	200	240	kHz
	Switching frequency	Rrt = 100 kΩ (1%)	400	480	560	kHz
	Maximum switching frequency	Rrt = 29 kΩ (1%)	1440	1600	1760	kHz
t_{on_min}	Minimum pulse width			20		ns
$RT_{_th}$	RT high threshold			2		V
	RT low threshold			0.8		V
$RT_{_delay}$	RT falling edge to PH rising edge delay	Measured at 500 kHz with RT resistor in series		66		ns
F_{SW_range}	Switching frequency range (RT mode set point and PLL mode)		200		1600	kHz
SW (SW PIN)						

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t_{on_min}	Minimum on-time	Measured at 90% to 90% of VIN, 25°C, Isw = 2 A	94	135	ns
t_{off_min}	Minimum off-time	BST-SW ≥ 3 V	0		ns
BST (BST PIN)					
BST_{UVLO}	BST-SW UVLO		2.1	3	V
SLOW START AND TRACKING (SS/TR PIN)					
I_{SS}	SS charge current		2.3		uA
V_{SS_FB}	SS to FB matching	V_{SS} = 0.4 V	29	60	mV

Note:
1) Guaranteed by design

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8 Typical Characteristics

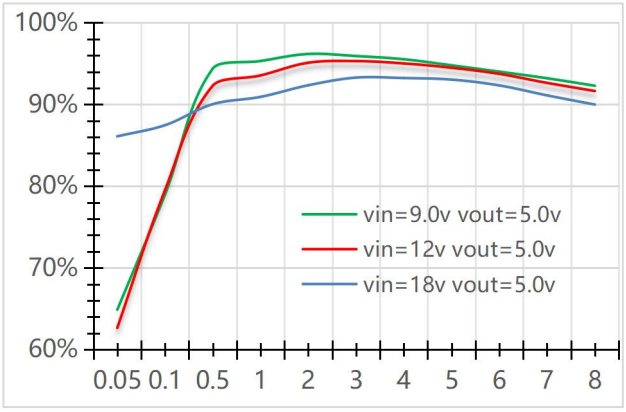


Fig. 8-1 Efficiency

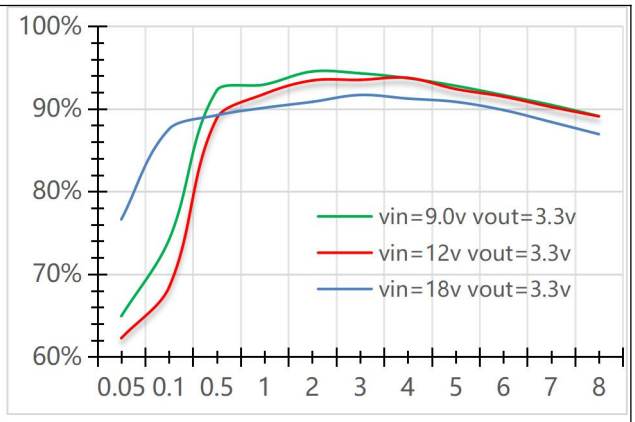
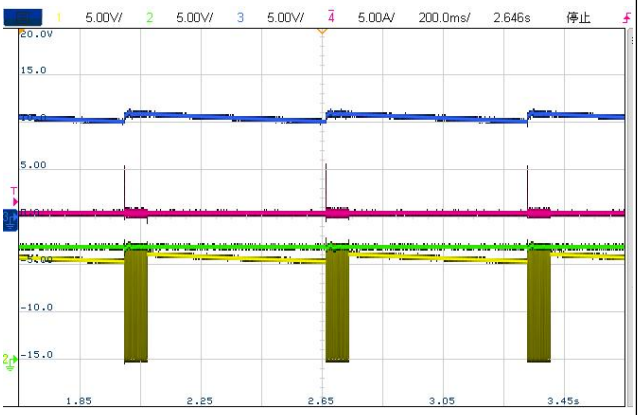
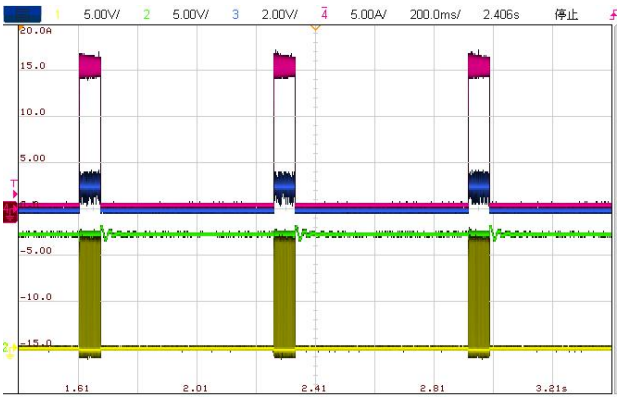


Fig. 8-2 Efficiency



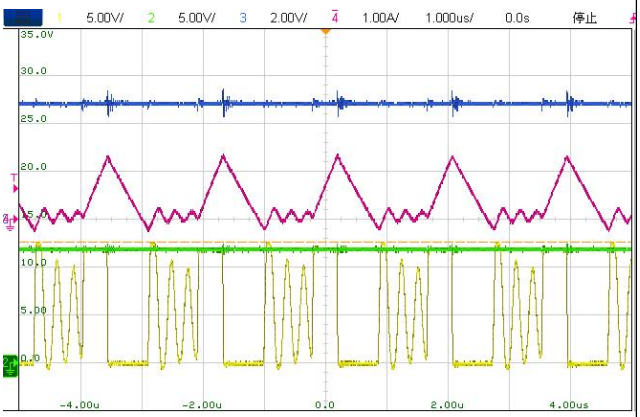
CH1:SW CH2:Vin CH3:Vout CH4:IL
Vin=12V Vout=5V

Fig.8-3 FB float OVP test



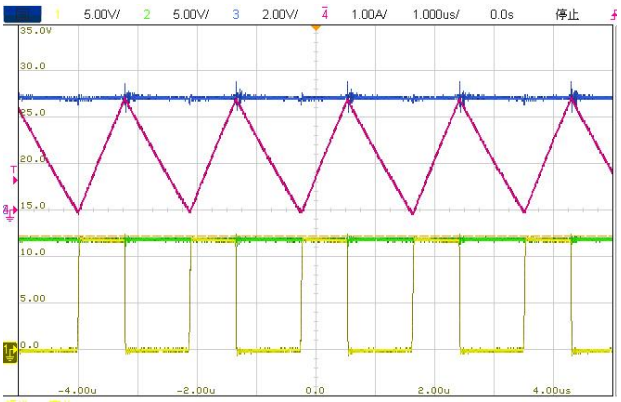
CH1:SW CH2:Vin CH3:Vout CH4:IL
Vin=12V Vout=5V

Fig.8-4 Short Circuit waveform



CH1:SW CH2:Vin CH3:Vout CH4:IL
Vin=12V Vout=5V

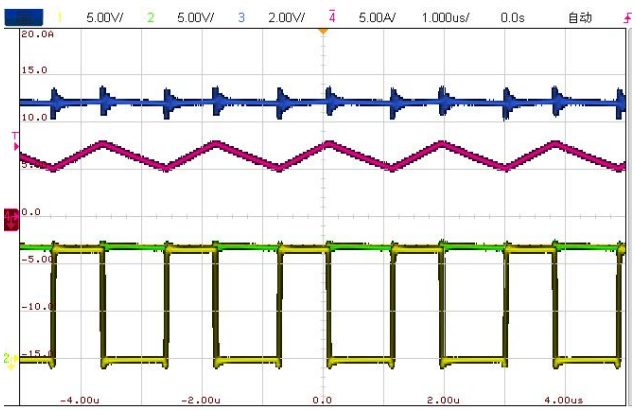
Fig.8-5 DCM Steady State waveform, Iout =0.3A



CH1:SW CH2:Vin CH3:Vout CH4:IL
Vin=12V Vout=5V

Fig.8-6 CCM Steady State waveform, Iout =1A

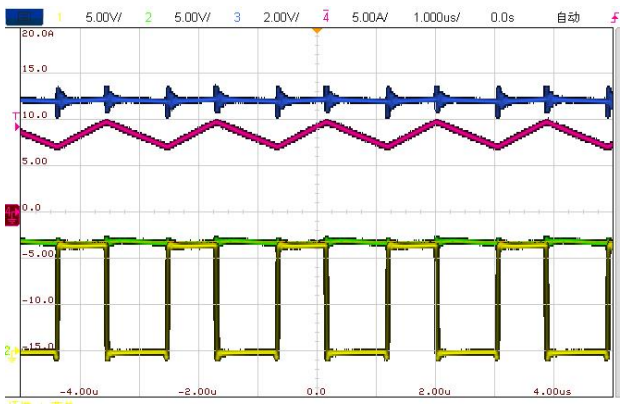
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CH1:SW CH2:Vin CH3:Vout CH4:IL

Vin=12V Vout=5V

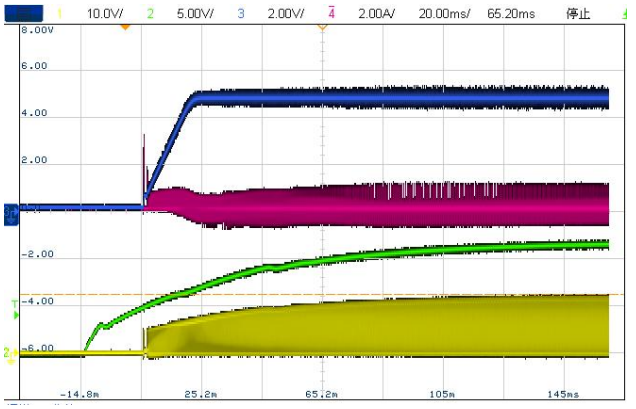
Fig.8-7 CCM Steady State waveform, Iout =6A



CH1:SW CH2:Vin CH3:Vout CH4:IL

Vin=12V Vout=5V

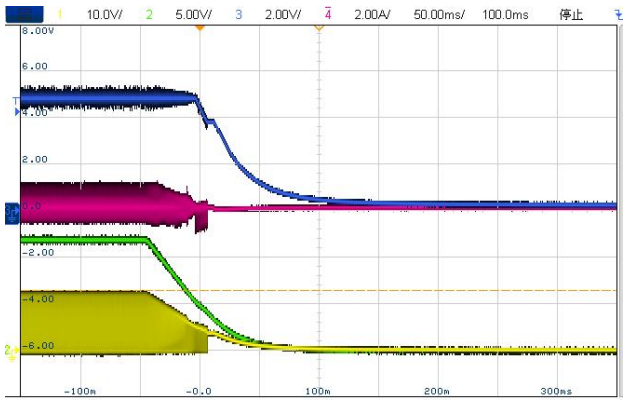
Fig.8-8 CCM Steady State waveform, Iout =6A



CH1:SW CH2:Vin CH3:Vout CH4:IL

Vin=12V Vout=5V

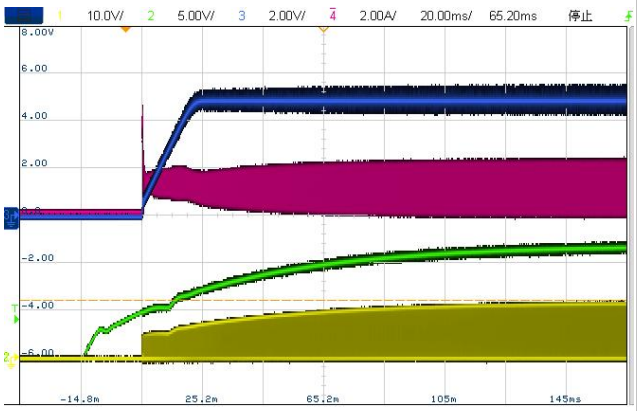
Fig.8-11 VIN Start up waveform, Iout =0A



CH1:SW CH2:Vin CH3:Vout CH4:IL

Vin=12V Vout=5V

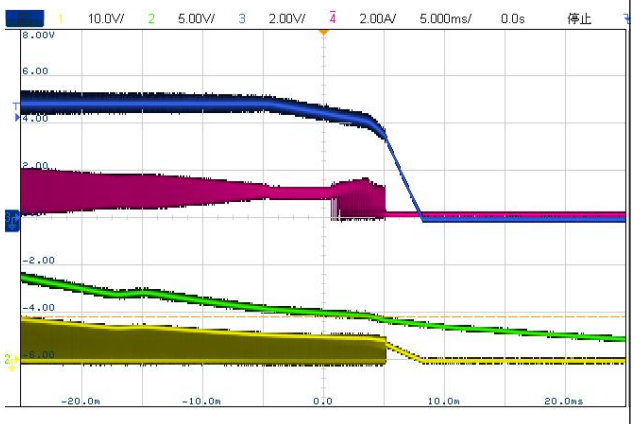
Fig.8-12 VIN Shut down waveform, Iout =0A



CH1:SW CH2:Vin CH3:Vout CH4:IL

Vin=12V Vout=5V

Fig.8-13 VIN Start up waveform, Iout =1A

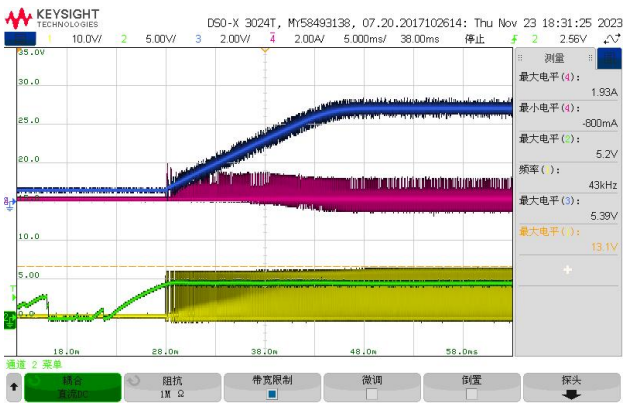


CH1:SW CH2:Vin CH3:Vout CH4:IL

Vin=12V Vout=5V

Fig.8-14 VIN Shut down waveform, Iout =1A

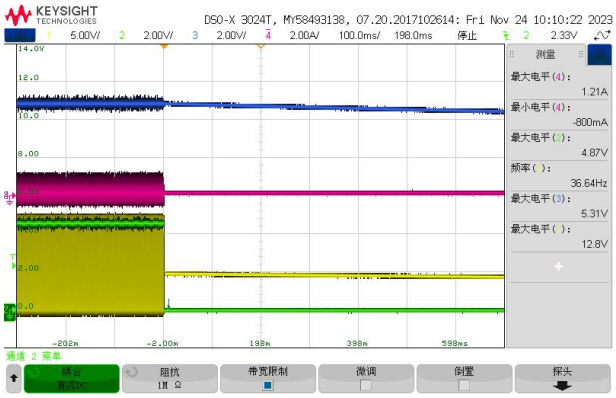
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CH1:SW CH2:EN CH3:Vout CH4:IL

Vin=12V Vout=5V

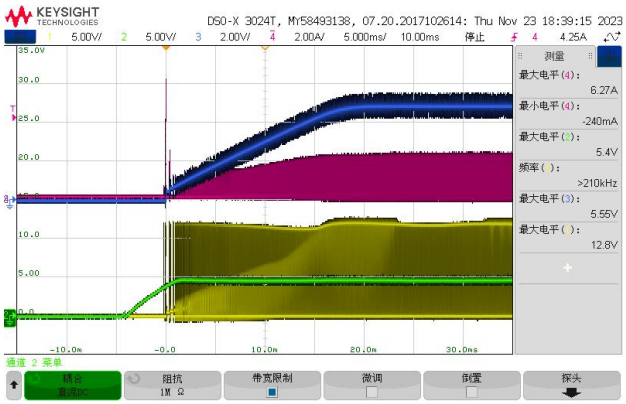
Fig.8-15 EN Start up waveform, Iout =0A



CH1:SW CH2:EN CH3:Vout CH4:IL

Vin=12V Vout=5V

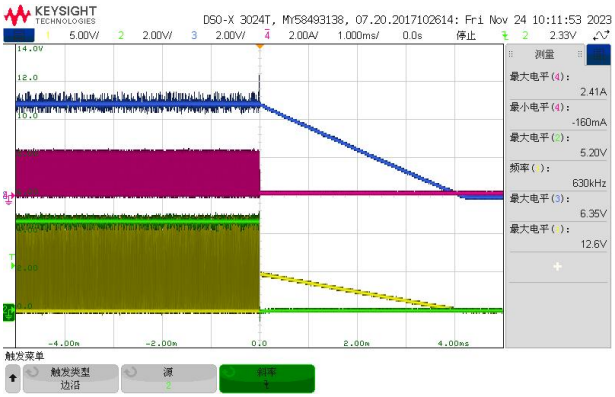
Fig.8-16 EN Shut down waveform, Iout =0A



CH1:SW CH2:EN CH3:Vout CH4:IL

Vin=12V Vout=5V

Fig.8-17 EN Start up waveform, Iout =1A



CH1:SW CH2:EN CH3:Vout CH4:IL

Vin=12V Vout=5V

Fig.8-18 EN Shut down waveform, Iout =1A

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9 Detailed Description

9.1 Overview

The device is a 17V, 6A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients, the device implements a constant frequency peak current mode control that also simplifies external frequency compensation. The wide switching frequency of 200kHz to 1600kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor-to-ground on the RT pin. The device also has an internal phase lock loop (PLL) controlled by the RT pin that can be used to synchronize the switching cycle to the falling edge of an external system clock.

The device has been designed for safe monotonic start-up into prebiased loads. The default start-up is when VIN is typically 4.5V. The EN pin can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. When the device is disabled, the supply current is typically less than 0.1μA.

The device has a power good comparator (PGOOD) with hysteresis which monitors the output voltage through the FB pin. The PGOOD pin is an open-drain MOSFET which is pulled low when the FB pin voltage is less than 91% or greater than 109% of the reference voltage Vref and asserts high when the FB pin voltage is 94% to 106% of the Vref.

The device is protected from output over voltage, overload, and thermal fault conditions. The device minimizes excessive output over voltage transients by taking advantage of the over voltage circuit power good comparator. When the over voltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the FB pin voltage is lower than 106% of the Vref. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections which help control the inductor current and avoid current runaway. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. The device is restarted under control of the slow-start circuit automatically when the junction temperature drops 10°C typically below the thermal shutdown trip point.

9.2 Functional Block Diagram

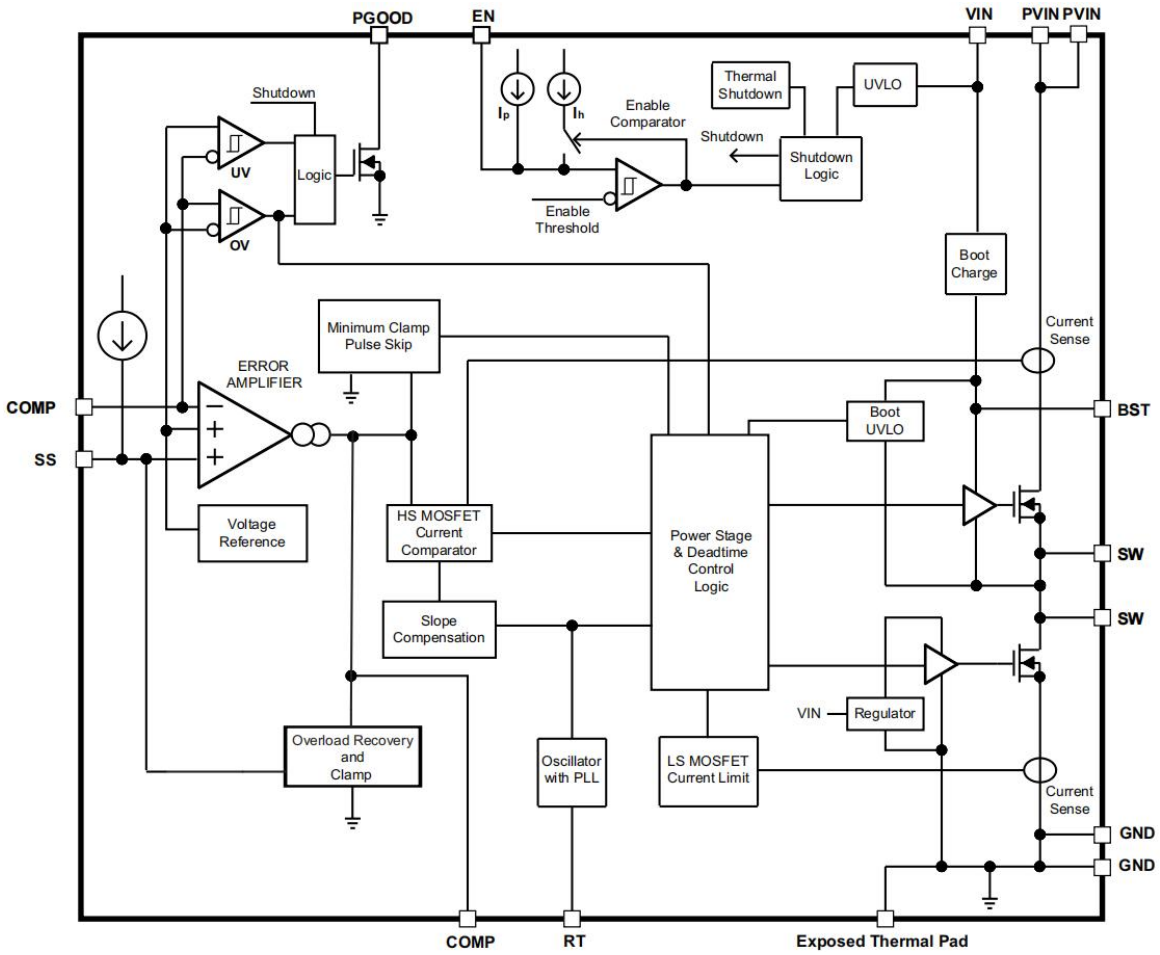


Fig. 9-2 Block Diagram

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9.3 Feature Description

9.3.1 Enable/UVLO

When EN is greater than 1.2V operating threshold, the control loop starts to work and regulate output to target voltage. When EN pin is below the standby threshold (1.0V typical), PL8106 stops working.

9.3.2 Fixed Frequency PWM Control

The device uses a adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches current reference generated by the COMP voltage level the high-side power switch is turned off and the low-side power switch is turned on.

9.3.3 AVIN and Power VIN Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power converter system.
If tied together, the input voltage for VIN and PVIN can range from 4.5V to 20V. If using the VIN separately from PVIN, the VIN pin must be between 4.5V and 20V, and the PVIN pin can range from as low as 2.5V to 20V. A voltage divider connected to the EN pin can adjust the either input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power up behavior.

9.3.4 Safe Start-Up into Prebiased Output

The device has been designed to prevent the low-side MOSFET from discharging a prebiased output. During monotonic prebiased start-up, the low-side MOSFET is not allowed to sink current until the SS pin voltage is higher than 1.4 V.

9.3.5 Slow Start(SS)

The device uses the lower voltage of the internal voltage reference or the SS pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS pin to ground implements a slow-start time. The device has an internal pull up current source of 2.3 μ A that charges the external slow-start capacitor. The calculations for the slow-start time (Tss, 10% to 90%) and slow-start capacitor (Css) are shown in the following equation:

$$t_{ss}(ms) = \frac{Css(nf) \times Vref(V)}{Iss(uA)}$$

When the input UVLO is triggered, the EN pin is pulled below 1.0V, or a thermal shutdown event occurs, the device stops switching and enters low current operation. At the subsequent power up when the shutdown condition is removed, the device does not start switching until it has discharged its SS/TR pin to ground ensuring proper soft-start behavior.

9.3.6 Frequency Setting (FREQ) and frequency dithering

The RT/CLK pin can be used to set the switching frequency of the device in two modes.
In RT mode, a resistor (RT resistor) is connected between the RT/CLK pin and GND. The switching frequency of the device is adjustable from 200 kHz to 1600 kHz by placing a maximum of 240kΩ and minimum of 29kΩ, respectively.

$$F_{SW}(kHz) = \frac{50000}{R_{FREQ}}(K\Omega)$$

In CLK mode, an external clock is connected directly to the RT/CLK pin. The device is synchronized to the external clock frequency with PLL.
The CLK mode overrides the RT mode. The device is able to detect the proper mode automatically and switch from the RT mode to CLK mode.

9.3.7 Power Good

The PGOOD pin is an open-drain output. When the FB pin is between 94% and 106% of the internal voltage reference the PGOOD pin pull down is deasserted and the pin floats. Recommends using a pull up resistor between the values of 10kΩ and 100kΩ to a voltage source that is 5.5V or less. The PGOOD is in a defined state when the VIN input voltage is greater than 1V but with reduced current sinking capability. The PGOOD achieves full current sinking capability when the VIN input voltage is above 4.5V.
The PGOOD pin is pulled low when FB is lower than 91% or greater than 109% of the nominal internal reference voltage. Also, if the PGOOD is pulled low and the input UVLO or thermal shutdown are asserted, the EN pin is pulled low or the SS pin is set below 1.4V.

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9.3.8 Output Over voltage Protection (OVP)

The device incorporates an output over voltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. When the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

9.3.9 Over current Protection

The device is protected from over current conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

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10 Applications and Implementation

The PL8106 device is a highly-integrated, synchronous, step-down, DC-DC converter. This device is used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 6A.

10.1 Operating Frequency

The first step is to decide on a switching frequency for the regulator. There is a trade-off between higher and lower switching frequencies. Higher switching frequencies may produce a smaller solution size using lowervalued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which hurt the efficiency and thermal performance of the converter. In this design, a moderate switching frequency of 480 kHz is selected to achieve both a small solution size and a high-efficiency operation.

10.2 Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The inductor current ripple ∆ IL is typically set to 20% to 40% of the maximum inductor current in the boost region at $V_{IN(MIN)}$.

For a given ripple, the inductance terms in continuous mode are as follows:

$$L_{BUCK} > \frac{V_{OUT}*(V_{IN(MAX)}-V_{OUT})*1000}{f*\Delta I_L*V_{IN(MAX)}}\ uH$$

where: f is operating frequency, kHz

$V_{IN(MIN)}$ is minimum input voltage, V

$V_{IN(MAX)}$ is maximum input voltage, V

V_{OUT} is output voltage, V

ΔI_L is maximum inductor ripple current, A, usually select 20~40% maximum output current.

10.3 CIN and COUT Selection

Input capacitor CIN is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current, input RMS current is given by:

$$I_{CIN}=I_{OUT(MAX)}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

This input current has a maximum at $V_{IN} = 2V_{OUT}$, $I_{CIN(MAX)} = I_{OUT(MAX)}/2$.
The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage.
V_{OUT} ripple is given by:

$$\Delta V_{OUT}\leq\Delta I_L*\left(ESR+\frac{1}{8*f*C_{OUT}}\right)$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

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11 PCB Layout

11.1 Guideline

The basic PCB board layout requires a separation of sensitive signal and power paths. If the layout is not carefully done, the regulator could suffer from the instability or noise problems. The checklist below is suggested that be followed to get good performance for a well-designed board:

1. The top layer contains the main power traces for VIN, VOUT. Also, on the top layer are connections for the remaining pins of the PL8106 and a large top-side area filled with ground.
2. The top layer ground area must be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the PL8106 device to provide a thermal path from the exposed thermal pad land to ground.
3. The GND pin must be tied directly to the power pad under the IC and the power pad.
4. For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
5. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.
6. To help eliminate these problems, the PVIN pin must be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric.
7. Take care to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections.
8. The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric.
9. Make sure to connect this capacitor to the quite analog ground trace rather than the power ground trace of the PVIN bypass capacitor.
10. Since the PH connection is the switching node, the output inductor must be placed close to the SW pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
11. The output filter capacitor ground must use the same power ground trace as the PVIN input bypass capacitor.
12. Try to minimize this conductor length while maintaining adequate width.
13. The small signal components must be grounded to the analog ground path as shown.
14. All sensitive analog traces and components such as FB, RT and COMP must be placed away from high-voltage switching nodes such as SW, BST and the output inductor to avoid noise coupling.
15. The output voltage sense trace must be connected to the positive terminal of one output capacitor in the design, with the best high frequency characteristics. The output voltage will be most tightly regulated at the voltage sense point.
16. The RT pin is sensitive to noise so the RT resistor must be placed as close as possible to the IC and routed with minimal lengths of trace.
17. The additional external components can be placed approximately as shown.
18. It may be possible to obtain acceptable performance with alternate PCB layouts, However this layout has been shown to produce good results and is meant as a guideline.

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11.2 Application Examples

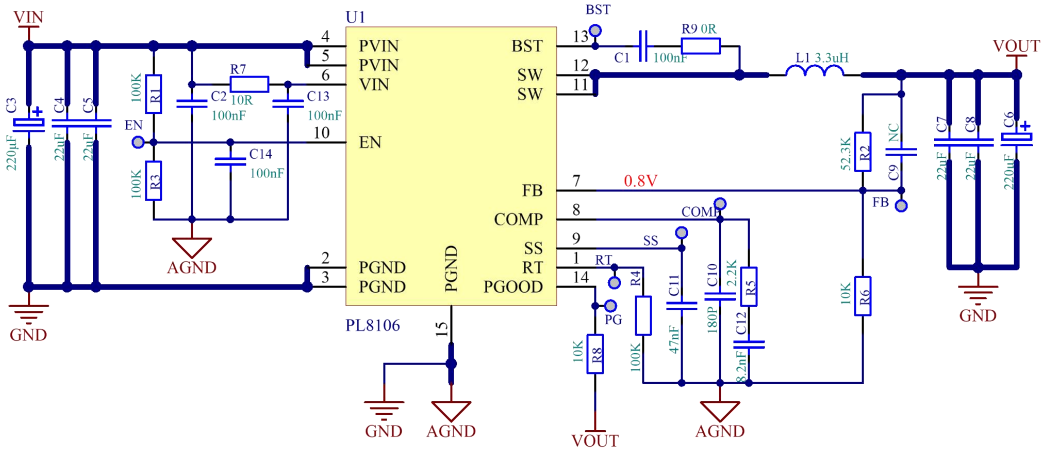


Fig. 11-2-1 Schematic

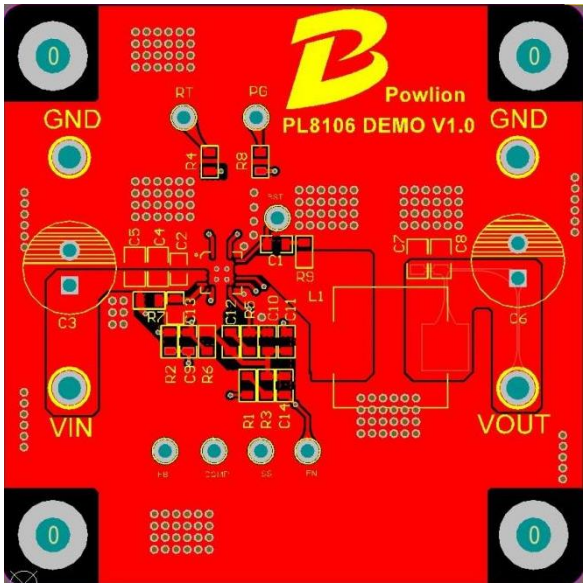


Fig. 11-2-2 Top Layer

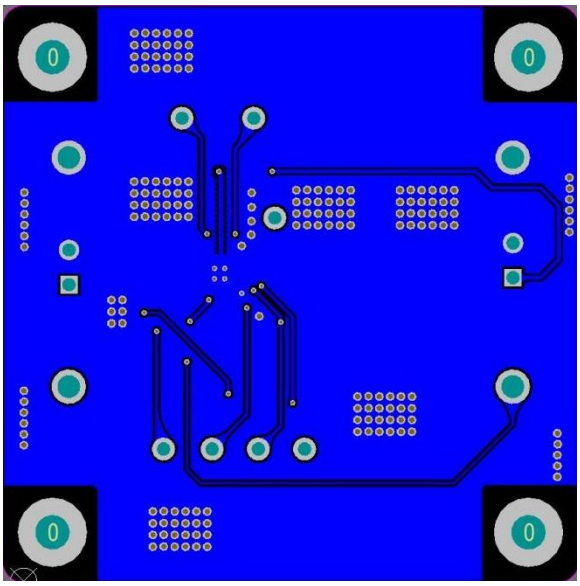
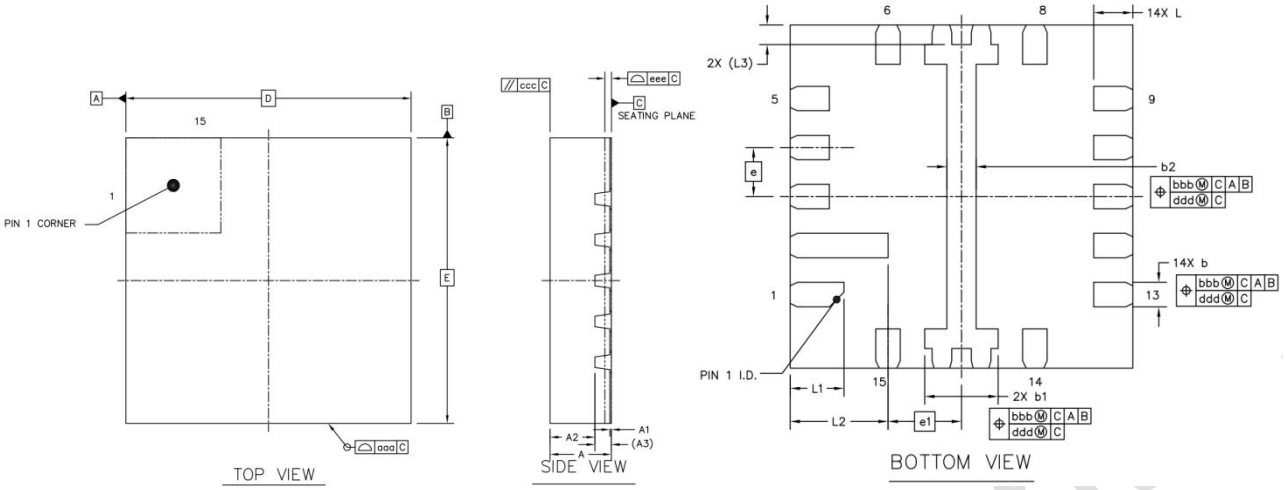


Fig. 11-2-3 Bottom Layer

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12 Packaging Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
		b1	0.7	0.75	0.8
		b2	0.25	0.3	0.35
BODY SIZE	X	D		3.5 BSC	
	Y	E		3.5 BSC	
LEAD PITCH		e		0.5 BSC	
		e1		0.75 BSC	
LEAD LENGTH		L	0.3	0.4	0.5
		L1	0.45	0.55	0.65
		L2	0.9	1	1.1
LEAD EDGE TO PKG EDGE		L3		0.2 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	

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