40V, 3.5A Monolithic Step-Down Switching Regulator

1 Features

- 3.5A continuous output current capability
- Up to 98% duty
- 4.6V to 33V wide operating input range
- Integrated 40V, 80mΩ high side and 40V, 50mΩ low side power MOSFET switches
- Up to 97% efficiency
- CV/CC Mode control (Constant voltage and constant current).
- Internal Soft-Start limits the inrush current at turn-on
- Fixed 160KHz Switching Frequency
- Internal compensation to save external components
- Pulse Skipping Mode to Achieve High Light Load Efficiency
- Frequency jittering to ease EMI Issue
- Peak Current-Mode Control
- Cycle-by-Cycle Over Current Protection
- Input over-voltage protection
- Output Over-Voltage Protection
- Output short protection
- Over-Temperature Protection
- Available in ESOP8 Package

2 Applications

- 9-V, 12-V and 24-V Distributed Power Systems
- Consumer Applications Such as Home Appliances,Set-Top Boxes, CPE Equipment, LCD Displays, Peripherals, and Battery Chargers
- Industrial and Car Entertainment Power Supplies

3 Description

The PL82051 is a monolithic synchronous buck regulator with wide operating input voltage range from 4.6 to 33V. Current mode control with internal slope compensation is implemented to reduce component count.
PL82051 also features a light load pulse skipping mode, which allows for a power loss reduction from the input power supply to the system at light loading.
Frequency spread spectrum operation is introduced for EMI reduction.
A cycle-by-cycle current limit with frequency fold back protects the IC at over loading condition.

4 Typical Application Schematic

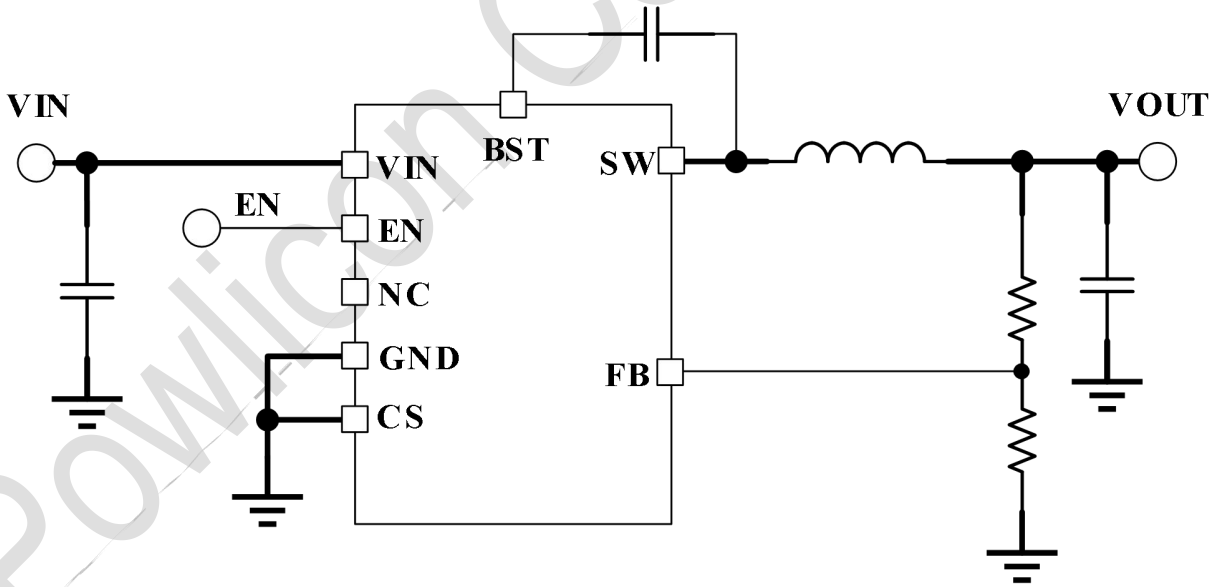


Fig. 1 Application Schematic

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5 Pin Configuration and Functions

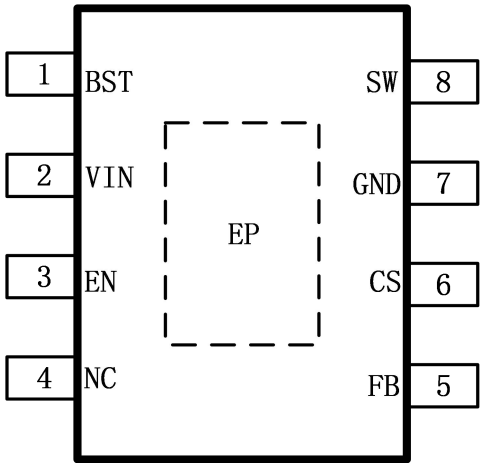


Fig. 2Pin-Function

Pin		Description
Number	Name	
1	**BST**	Boot-Strap pin Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver.
2	**VIN**	Power Input. VIN supplies the power to the IC. Supply VIN with a 4.6V to 33V power source. Bypass VIN to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors close to VIN and GND pins.
3	**EN**	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. EN pin is pulled to VIN internally by a larger resistor.
4	**NC**	No connect
5	**FB**	Output voltage feedback pin
6	**CS**	Current loop to configure load current limit and line drop compensation.
7	**GND**	Ground
8	**SW**	Power Switching pin. Connect this pin to the switching node of inductor.
	EP	Ground

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6 Device Marking Information

Order Information	Label Part NO.	Package	Package Qty	Top Marking
PL82051	PL82051IES08A	ESOP-8	4000	82051 RAAYMD

PL82051: Part Number
RAAYMD RAA: Lot Number. YMD: Package Date Code

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7 Specifications

7.1 Absolute Maximum Ratings(Note1)

Symbol	Description	Rating	Unit
VIN	VIN to GND Voltage	–0.3 to +40	V
BST	BST to SW Voltage	-0.3 to 6.5	V
SW	SW to GND Voltage	–0.3 to +40	V
Others	EN, FB,CS Voltage	-0.3 to +6.5	V

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+150	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model		2	kV

7.3 Recommended Operating Conditions (Note 2)

Symbol	Description	Rating	Unit
VIN	VIN Voltage	5 to +33	V
SW	SW Voltage	0 to +33	V
BST	BST Voltage	0 to SW+5	V
EN	EN Voltage	0 to 5	V
FB	FB voltage	0 to 5	V
Others	CS Voltage	0 to 5	V
T_A	Operating Ambient Temperature Range	-40 to +125	°C

7.4 Thermal Information(Note 3)

Symbol	Description	ESOP8	Unit
θ_{JA}	Junction to ambient thermal resistance	56	°C/W
θ_{JC}	Junction to case thermal resistance	45	

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1” square of 1 oz copper.

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7.5 Electrical Characteristics

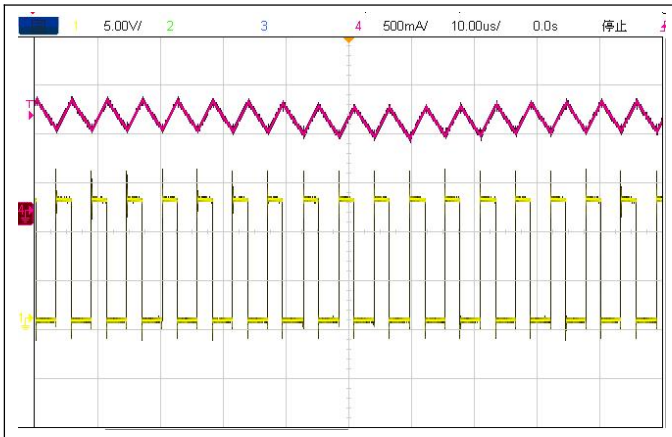
VIN = 12 V, TJ = - 40 °C to 125 °C , Typical values are at TJ = 25 °C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Type	Max	Unit
SUPPLY VOLTAGE (VIN)						
V_{IN_max}	Buck input standoff voltage		40			V
V_{IN}	Buck input voltage range		4.6		33	V
V_{IN_UVLO}	VIN UVLO voltage	VIN rising		4.6		V
		VIN falling		4.1		V
V_{IN_OVP}	VIN over voltage	VIN rising		33		V
		VIN falling		30		V
I_Q	VIN Shutdown Current	V_{EN} = 0, V_{IN} = 12V		10		uA
CONTROL LOOP						
F_{buck}	Buck switching frequency range		120	160	200	kHz
fjitter	Frequency spread spectrum in percentage ofF_{buck}			±6		%
FB	FB VOLTAGE		0.788	0.8	0.812	V
VOUT_OVP	OUTPUT Over-voltage threshold			1.1*FB		V
Dmax	Maximum Duty Cycle			98		%
Ton	Minimum On Time			100		ns
ILIMIT	Peak inductor current limit			6.5		A
MOSFET AND PROTECTION						
$R_{DS(ON)_H}$	High-Side Switch On-Resistance			80		mΩ
$R_{DS(ON)_L}$	Low-Side Switch On-Resistance			50		mΩ
Th_{sd}	Thermal Shutdown			160		℃
Th_{sdhys}	Thermal Shutdown Hysteresis			60		℃

Note:
4) Guaranteed by design, not tested in production

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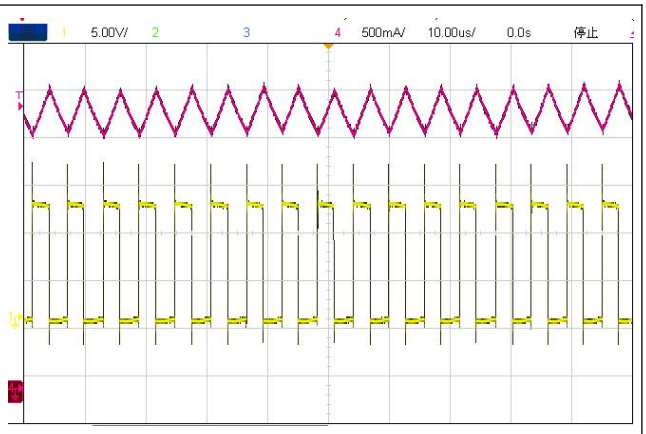
8 Typical Characteristics



CH1:SW CH4:IL

VIN=12V VOUT=5V

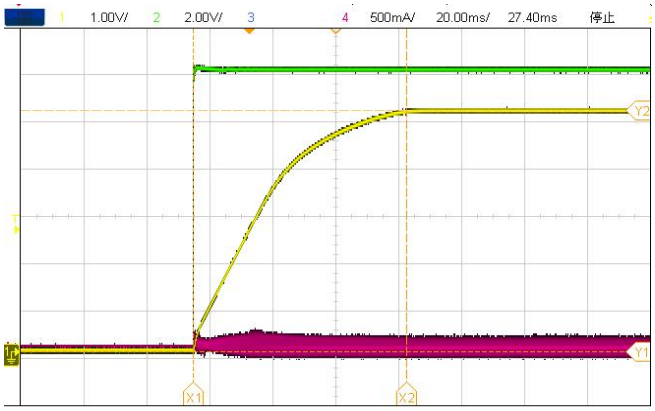
Fig. 3 Steady state waveform, IOUT=1A



CH1:SW CH4:IL

VIN=12V VOUT=5V

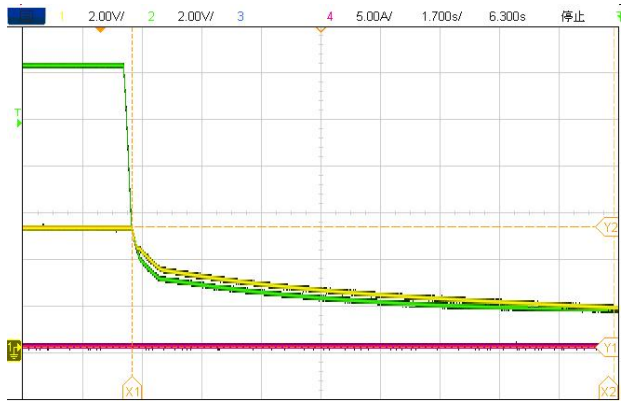
Fig. 4 Steady state waveform, IOUT=3.5A



CH1:VOUT CH3:VIN CH4:IL

VIN=12V VOUT=5V

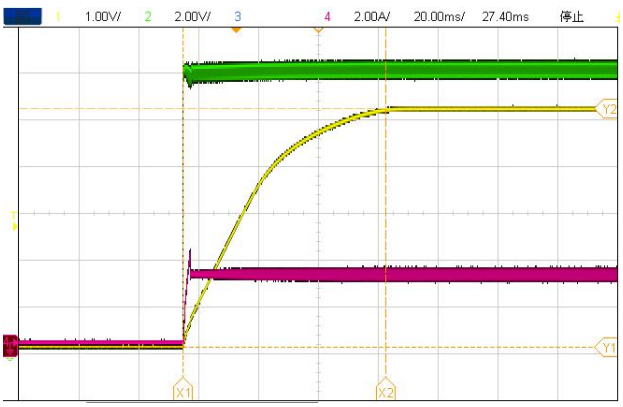
Fig. 5 Startup waveform, Iout = 0A



CH1:VOUT CH3:VIN CH4:IL

VIN=12V VOUT=5V

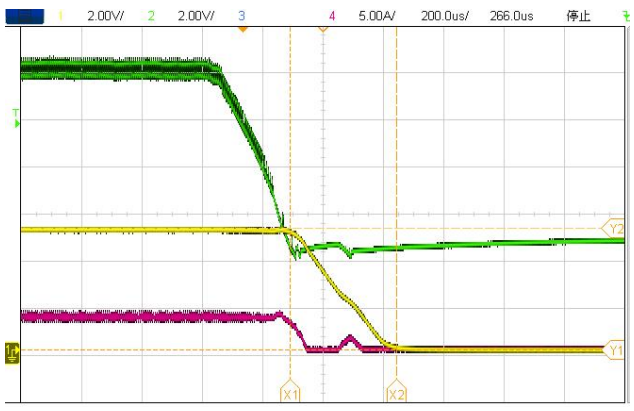
Fig. 6 Shutdown waveform, Iout = 0A



CH1:VOUT CH3:VIN CH4:IL

VIN=12V VOUT=5V

Fig. 7 Startup waveform, Iout = 3.5A

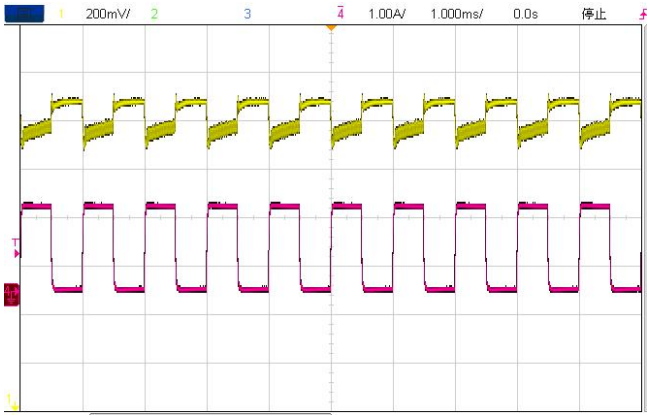


CH1:VOUT CH3:VIN CH4:IL

VIN=12V VOUT=5V

Fig. 8 Shutdown waveform, Iout = 3.5A

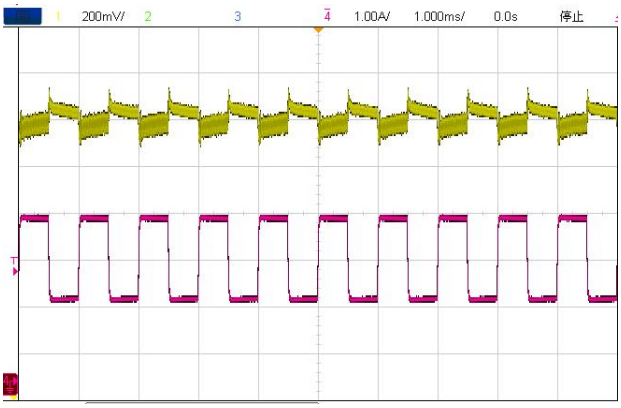
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CH1:VOUT CH4:IOUT

VIN=12V ,VOUT=5V 0A-1.75A, 0.25A/us, 1KHZ, Duty50%

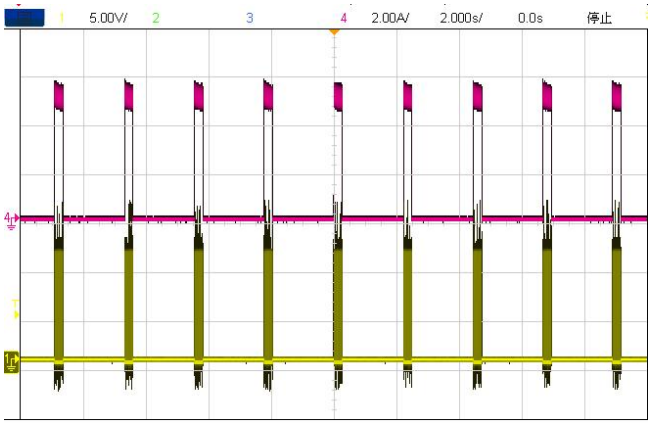
Fig. 9 Load Transient waveform



CH1:VOUT CH4:IOUT

VIN=12V ,VOUT=5V 1.75A-3.5A, 0.25A/us, 1KHZ, Duty50%

Fig. 10 Load Transient waveform



CH1:SW CH4:IL

VIN=12V VOUT=5V

Fig. 11 Short Circuit waveform

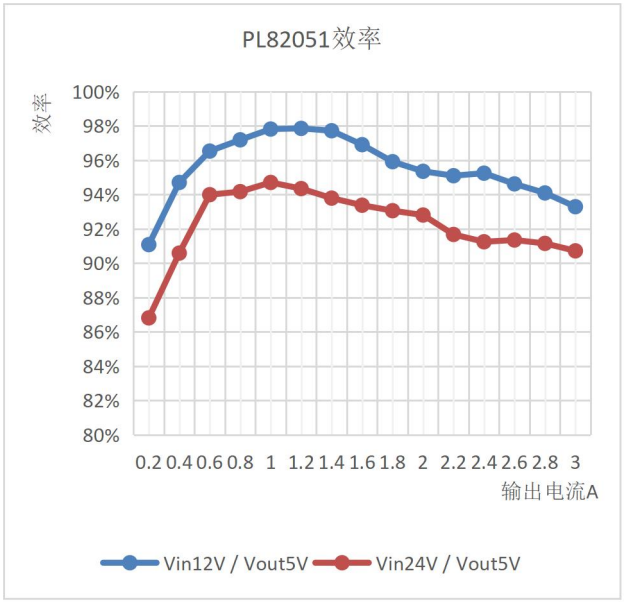


Fig. 12 efficiency curve

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9. Detailed Description

9.1 Overview

The PL82051 is a 40V, 3.5A, step-down (buck) converter with an integrated N-channel MOSFET. To improve performance during line and load transients, the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design.

The PL82051 starts switching at VIN equal to 4.6 V. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BST to SW pins. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V typically. To improve the efficiency at light load conditions, the PL82051 enters a special pulse skipping mode. The frequency foldback reduces the switching frequency during startup and over current conditions to help control the inductor current. The thermal shut down gives the additional protection under fault conditions.

9.2 Functional Block Diagram

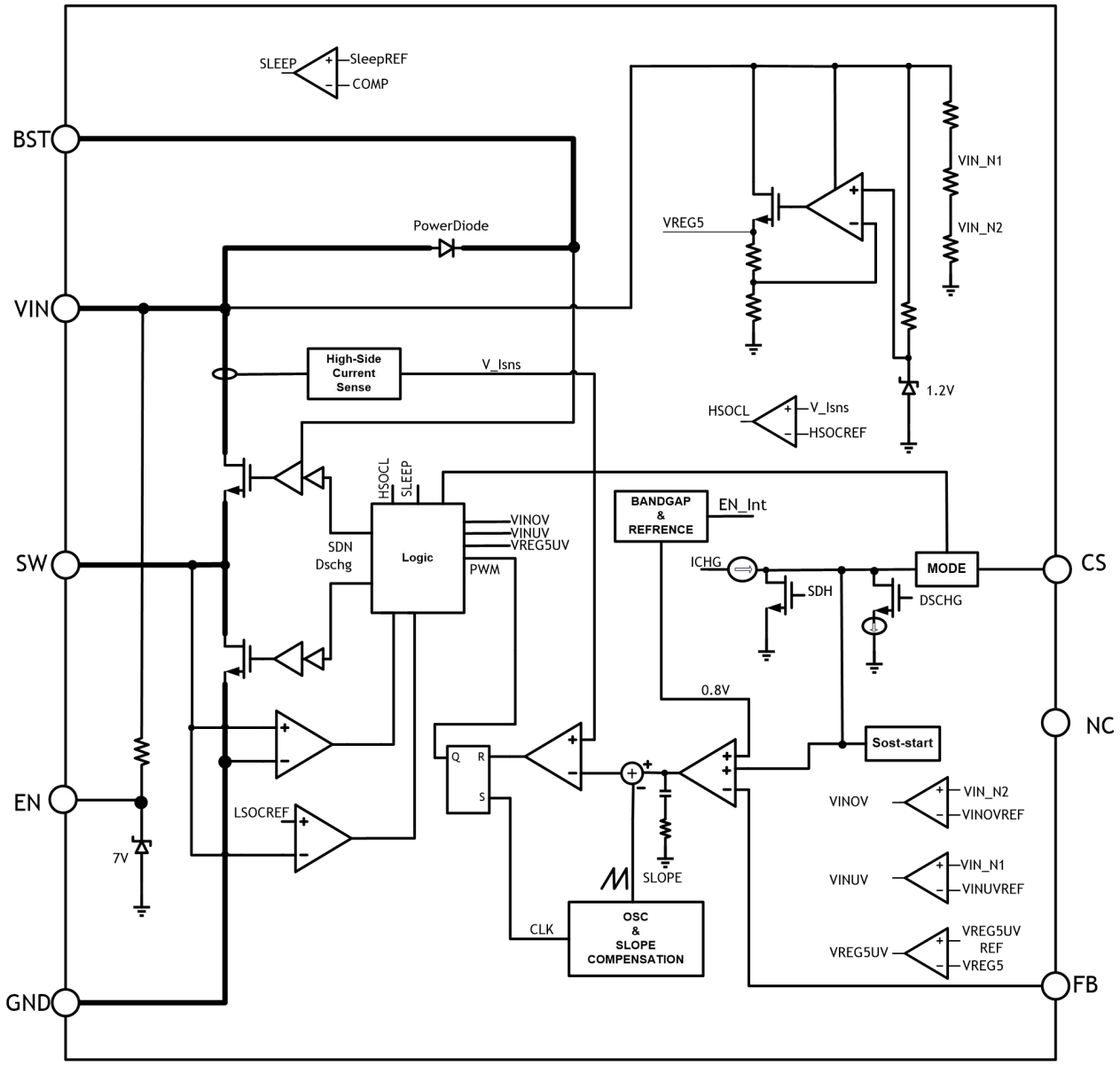


Figure 11 PL82051 Diagram

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9.3 Feature Description

9.3.1 CC/CV control mode and average load current limiting

PL82051 has a CC/CV control mode. The load current is sensed . When average load current is high enough, constant-current loop will be dominant and limit the average load current to a value configured by resistor on CS pin. The Relationship is below

Iout=45mv/R . The typical R is 10mΩ.

9.3.2 Setting Output Voltage

The voltage reference system produces a ±1.5% initial accuracy voltage reference by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.8 V.

$$V_{out}=V_{ref}\times\frac{R_1+R_2}{R_2}$$

9.3.3 Bootstrap Voltage (BST)

The PL82051 has an integrated boot regulator and requires a 0.1-μF ceramic capacitor between the BST and SW pins to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the PL82051 is designed to operate at 98% duty cycle as long as the BST to SW pin voltage is greater than 2.1 V typically.

9.3.4 Line drop compensation

When USB charging cable line is long and resistance is high, there will be some significant voltage drop on the cable. Portable device will see much lower input voltage. If the voltage across the load input terminals is too low, it will affect the charge time for the load. It is recommended to adjust the output voltage of charger to compensate this voltage drop. PL82051 has an excellent configurable line drop compensation feature. The line drop compensation value can be programmed by the top feedback resistor R1 in Fig 1. The value can be roughly calculated as equation below:

$$V_{LineDrop}=\frac{I_{Load}*R_{SNS}*15}{67K}*R1$$

I_{Load} is the load current. R_{SNS} is the programming resistor on CS pin. R1 is the top output sensing resistor.

9.3.5 Error Amplifier

The PL82051 has a transconductance amplifier for the error amplifier. The error amplifier compares the FB voltage to the internal effective voltage reference presented at the input of the error amplifier.

9.3.6 Spread Spectrum

In order to reduce EMI, PL82051 introduces frequency spread spectrum. The jittering span is ±6% of the switching frequency .

9.3.7 Peak Current Mode Control

PL82051 employs peak current mode control. The output voltage is sensed by an internal feedback resistor string on VOUT pin and fed to an internal error amplifier. The output of error amplifier will compare with high side current sense

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signal by an internal PWM comparator. When the second signal is higher than the first one, the PWM comparator will generate a turn-off signal to turn off high side switch. The output voltage of error amplifier will increase or decrease proportionally with the output load current. PL82051 has a cycle-by-cycle peak current limit feature inside to help maintain load current in a safe region.

9.3.8 Enable

PL82051 can be enabled by EN pin. EN pin internal threshold is set at 1.2V. EN pin has been pulled up inside. Customer can also adjust the startup voltage at input pin by this EN pin through resistor divider.

9.3.9 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. When the junction temperature drops below 100°C, IC will start to work again.

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10 Application and Implementation

10.1 Inductor selection

An inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 25% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s\times\Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, $f_S$is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum peak current. The peak inductor current can be calculated by:

$$I_{L_P}=I_{load}+\frac{V_{OUT}}{2\times f_s\times L}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{load} is the load current.

The choice of inductor material mainly depends on the price vs. size requirements and EMI constraints.

10.2 Input capacitors selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C_{IN}) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at V_{IN} = 2×V_{OUT}, where:

$$I_{CIN}=\frac{I_{load}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN}=\frac{I_{load}}{f_s\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

C_{IN} is the input capacitance.

10.3 Output capacitors selection

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended.

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Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_s\times C_{OUT}}\right)$$

Where L is the inductor value, R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor and C_{OUT} is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_s^{2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulator. PL8329Bis optimized for a wide range of capacitance and ESR values.

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11 PCB Layout

11.1 Guideline

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R_1 and R_2, should be kept close to FB pin. V_{out} sense path should stay away from noisy nodes, such as SW and BST signals and preferably through a layer on the other side of shielding layer.
2. The input bypass capacitor C_1 and C_2 must be placed as close as possible to the V_{IN} pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the V_{IN} pin to reduce the high frequency injection current.
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor, C_{OUT} should be placed close to the junction of L. The L and C_{OUT} trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. The ground connection forC_1, C_2 and C_3, C_4 should be as small as possible and connect to system ground plane at only one spot (preferably at the C_{OUT} ground point) to minimize injecting noise into system ground plane.
6. Place current sense resister R3 as near as possible to the chip and stay away from noisy nodes such as SW, BST.

11.2Application Examples

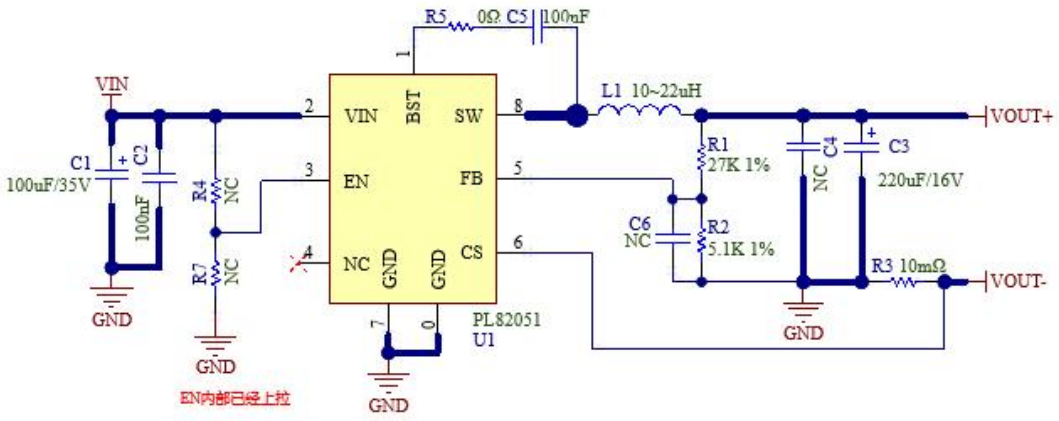


Fig. 11.2-1 Application Schematic

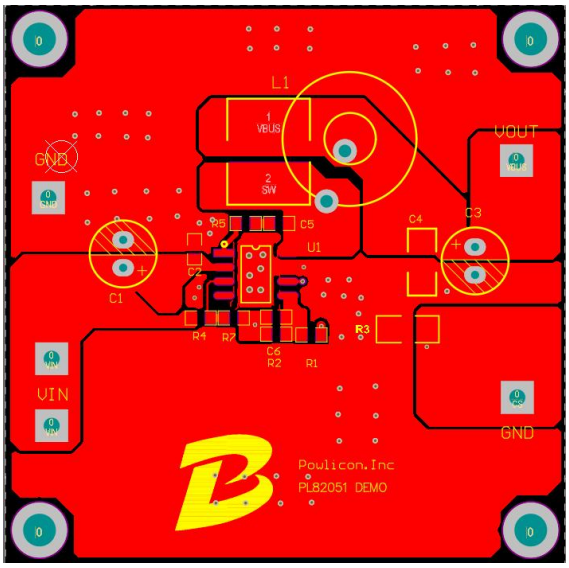


Fig. 11.2-2 Top Layer

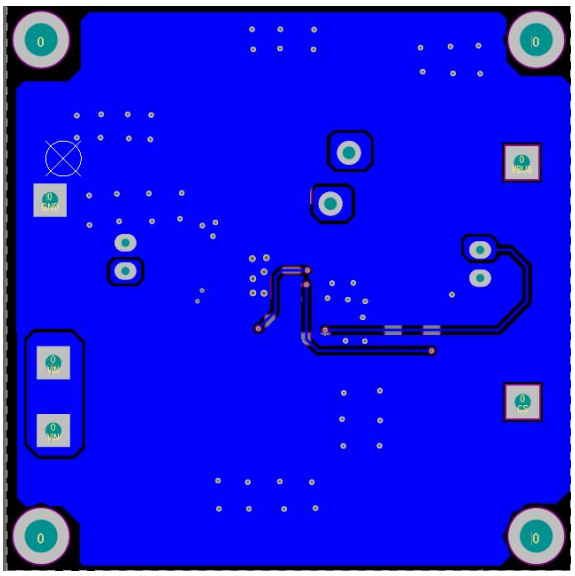
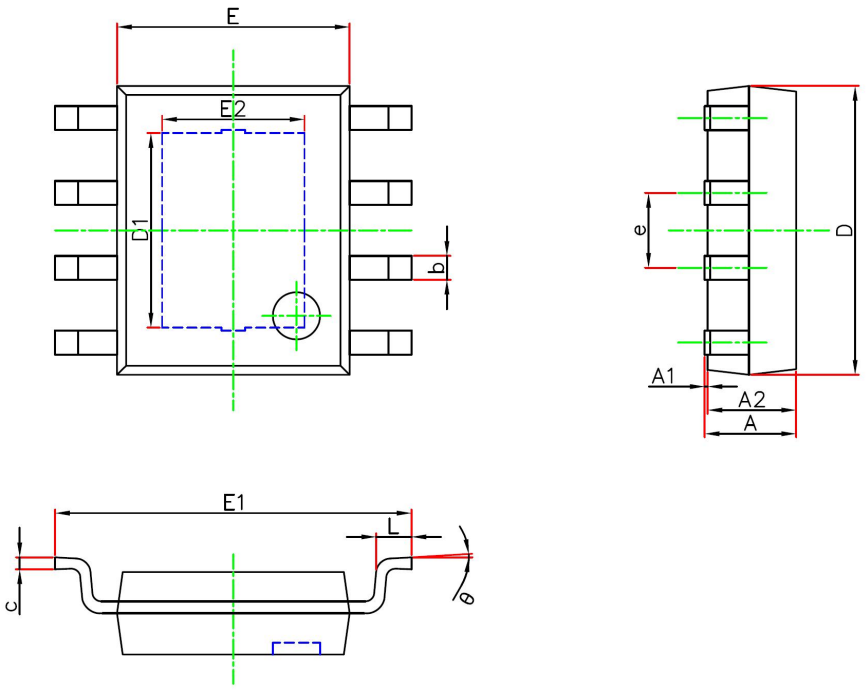


Fig. 11.2-3 Bottom Layer

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12 Packaging Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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