36V, 3.1A Monolithic Step-Down Switching Regulator

1 Features

- 3.1A continuous output current capability
- 6.5V to 36V wide operating input range with input Over Voltage Protection
- Integrated 36V, 79mΩ high side and 36V, 62mΩ low side power MOSFET switches
- Up to 95% efficiency
- Programmable Soft-Start limits the inrush current at turn-on
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 300KHz Switching Frequency
- Input Under-Voltage Lockout
- Input over-voltage protection to protect device from working in high voltage and high current condition
- Output Over-Voltage Protection
- Output short protection with both high side current limit and low side current limit to protect the device in hard short
- Over-Temperature Protection
- Thermally Enhanced ESOP-8 Package

2 Applications

- Set-Top-Box
- Televisions
- DVD, LCD Displays
- OLPC, Netbook
- Datacom, XDSL modems
- Distributed Power Systems
- USB car charger
- Portable charging device
- General purpose

3 Description

PL8332G is a monolithic 36V, 3.1A step-down switching converter. PL8332G integrates a 36V 79mΩ high side and a 36V, 62mΩ low side MOSFETs to provide 3.1A continuous load current over a 6.5V to 36V wide operating input voltage with 33V input over voltage protection. Peak current mode control provides fast transient responses and cycle-by-cycle current limiting. Programmable soft-start prevents inrush current at power-up.

4 Typical Application Schematic

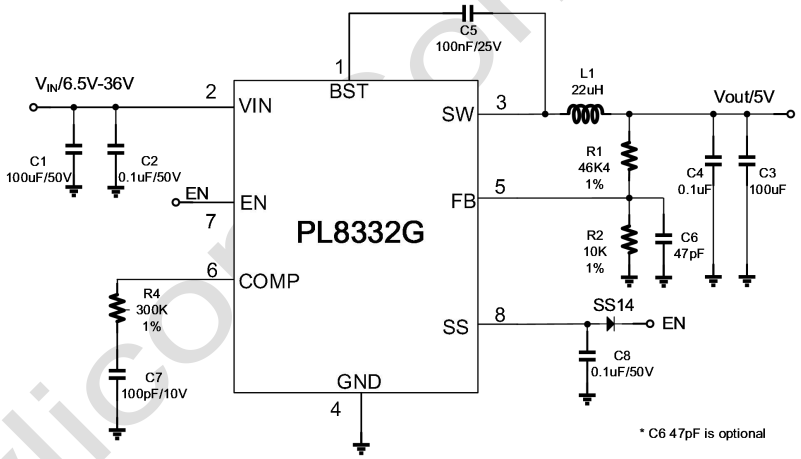


Fig. 1 Schematic

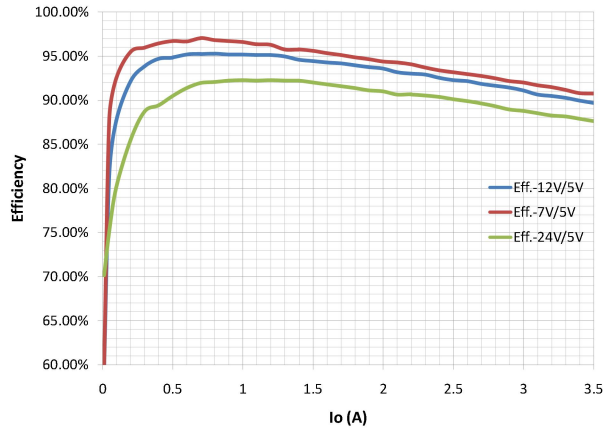
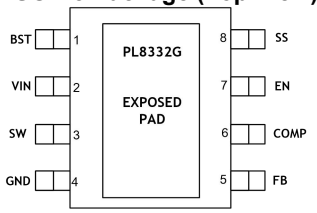


Fig. 2 Efficiency curve

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5 Pin Configuration and Functions

ESOP-8 Package (Top View)



Pin-Functions

Pin		Description
Number	Name	
1	BST	Boot-Strap pin Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver. Minimize BST and SW loop to reduce EMI.
2	VIN	Power Input. VIN supplies the power to the IC. Supply VIN with a 6.5V to 36V power source. Bypass VIN to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors, especially 0.1uF ceramic capacitor as close as possible to VIN and GND pins. Minimize 0.1uF capacitor, VIN pin, GND pin loop to reduce EMI and voltage spike on high side power device.
3	SW	Power Switching pin. Connect this pin to the switching node of inductor.
4	GND	Ground.
5	FB	Feedback Input. FB senses the output voltage. Connect FB with a resistor divider connected between the output and ground. FB is a sensitive node. Keep FB away from SW and BST pin. It is better to connect a 47pF capacitor on FB pin to filter out possible coupling from other noisy node such as SW, BST, and VIN.
6	COMP	Connect compensation network to make the converter work stably.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. EN pin is pulled to VIN internally by a larger resistor. No external resistor is needed to enable the part.
8	SS	This pin is used to program soft-start time, connect a cap to program soft-start time.
9	EPAD	Power ground and EPAD, for full load operation EPAD must been connected to PCB gnd.

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking	MSL
PL8332G	**PL8332GIES08**	**ESOP-8**	**4000**	**8332G RAAYMD**	**3**

PL8332G: Part Number
RAAYMD: RAA: Lot NO.; YMD: Package Date Co

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7 Specifications

7.1 Absolute Maximum Ratings(Note1)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	-0.3	36	V
	V_{EN} to GND	-0.3	6	
	V_{SS} to GND	-0.3	6	
	V_{FB} to GND	-0.3	6	
Output Voltages	V_{COMP} to GND	-0.3	6	V
	V_{BST} to V_{SW}	-0.3	6	
	V_{SW} to GND	-1	V_{IN}+ 0.3	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-55	150	°C
T_J	Junction Temperature		+160	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model		2	KV
	MM MACHINE MODE		400	V

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	6.5	30	V
	EN	-0.3	5	
	SS	-0.3	5	
	FB	-0.3	5	
Output Voltages	V_{OUT}	0.5	V_{IN}*D_{max}	V
Output Current	I_{OUT}	0	3.1	A
Temperature	Operating junction temperature range, T_J	-40	+125	°C

7.4 Thermal Information(Note 3)

Symbol	Description	ESOP-8	Unit
θ_{JA}	Junction to ambient thermal resistance	56	°C/W
θ_{JC}	Junction to case thermal resistance	45	

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

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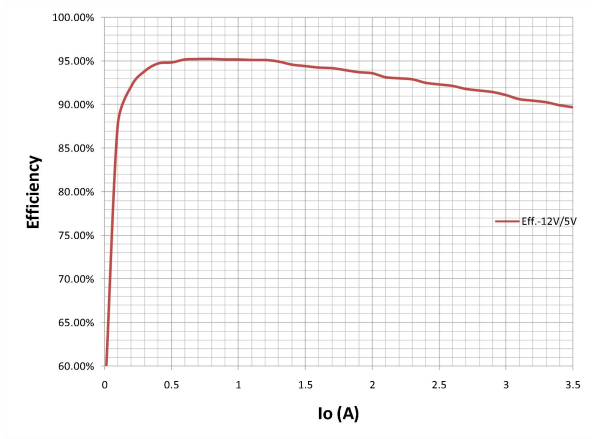
7.5 Electrical Characteristics (Typical at Vin = 12V, T_J=25°C, unless otherwise noted.)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
MOSFET						
$R_{DS(ON)_H}$	High-Side Switch On-Resistance	I_{OUT} = 1A, V_{OUT} = 3.3V		79		mΩ
$R_{DS(ON)_L}$	Low-Side Switch On-Resistance	I_{OUT} = 1A, V_{OUT} = 3.3V		62		mΩ
SUPPLY VOLTAGE (VIN)						
V_{UVLO_up}	Minimum input voltage for startup				6.5	V
V_{UVLO_down}				6.0		V
V_{UVLO_hys}				0.5		V
$I_{Q\text{-}NONSW}$	Operating quiescent current	V_{FB} =1.1V		1		mA
CONTROL LOOP						
F_{oscb}	Buck oscillator frequency			300		kHz
V_{FB}	Feedback Voltage	4.5V ≤ VIN ≤ 36V		0.9		V
V_{FB_OVP}	Feedback Over-voltage Threshold			0.99		V
D_{max}	Maximum Duty Cycle(Note 4)			94		%
T_{on}	Minimum On Time(Note 4)			100		ns
PROTECTION						
I_{ocl_hs}	Upper Switch Current Limit	Minimum Duty Cycle		5.9		A
I_{ocl_ls}	Lower Switch Current Limit	From Drain to Source		5.5		A
V_{inovp}	Input Over voltage protection			33		V
Th_{sd}	Thermal Shutdown(Note 4)			155		°C
Th_{sdhys}	Thermal Shutdown Hysteresis(Note 4)			15		°C
V_{IH}	EN High Voltage		1.2			V
V_{IL}	EN Low Voltage				1.1	V
I_{EN}	EN Input Current			1.6		uA
I_{chg_ss}	Soft-Start Charge Current			2.3		uA
I_{cmp_src}	Comp Source Current	V_{FB} = 1.0 V		5.2		uA
I_{cmp_snk}	Comp Sink Current	V_{FB} = 0.8 V		3.2		uA

Note:
4) Guaranteed by design, not tested in production.

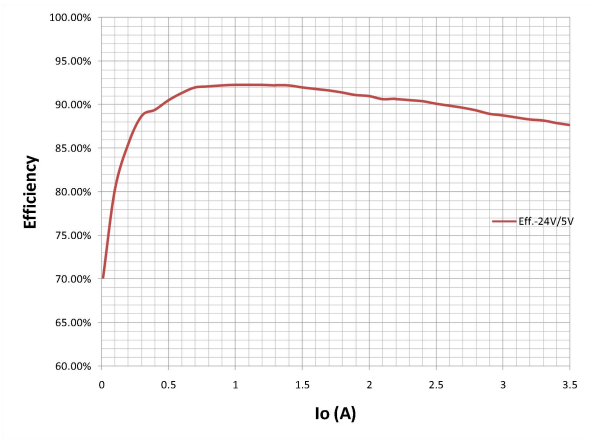
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8 Typical Characteristics



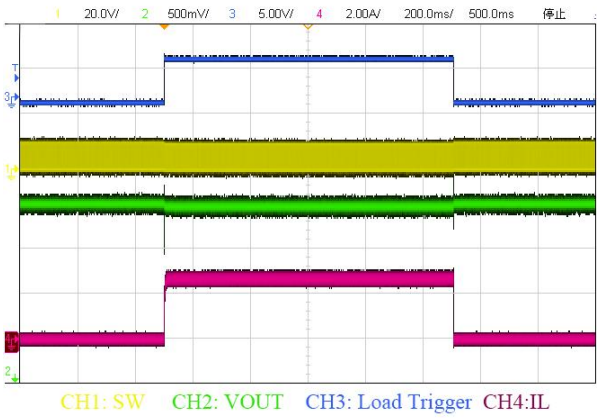
Vin = 12V, Vout = 5V

Fig. 3 Efficiency



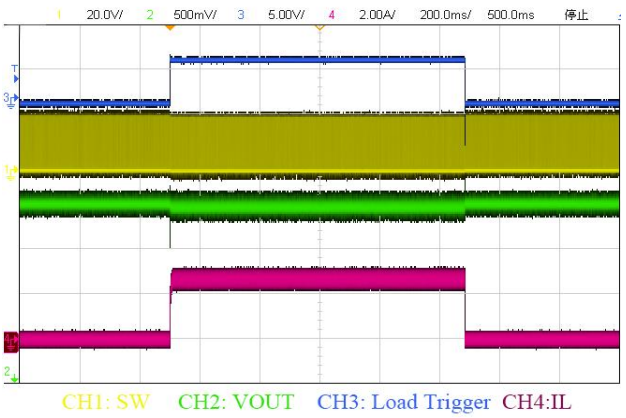
Vin = 24V, Vout = 5V

Fig. 4 Efficiency



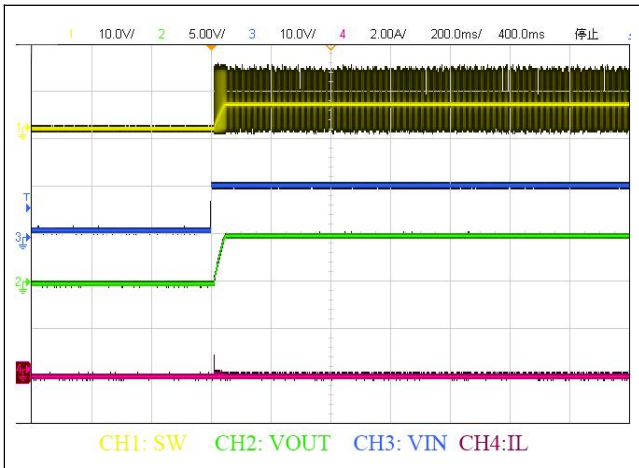
Vin = 12V, Vout = 5V

Fig. 5 Load transient 0.3A to 3A



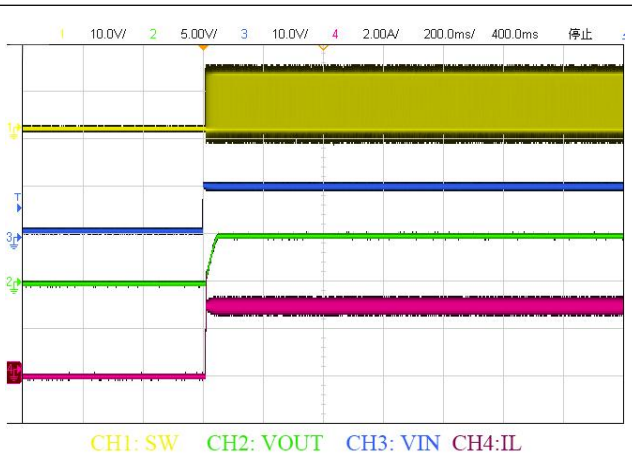
Vin = 24V, Vout = 5V

Fig. 6 Load transient 0.3A to 3A



Vin = 12V, Vout = 5V

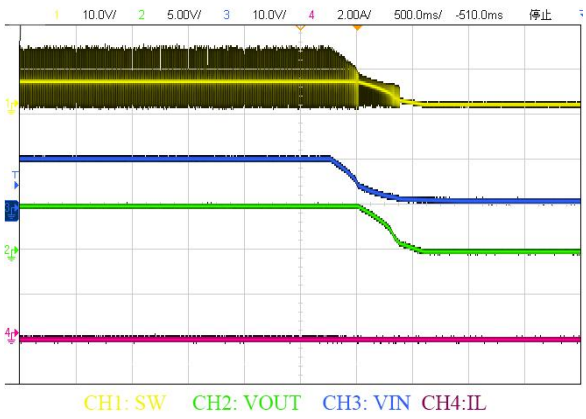
Fig. 7 Startup waveform, Iout = 0A



Vin = 12V, Vout = 5V

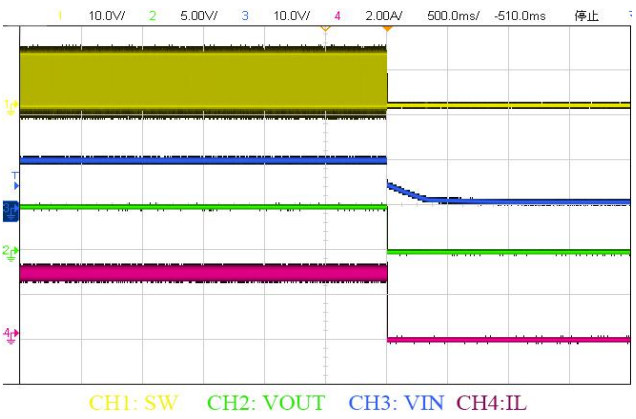
Fig. 8 Startup waveform, Iout = 3A

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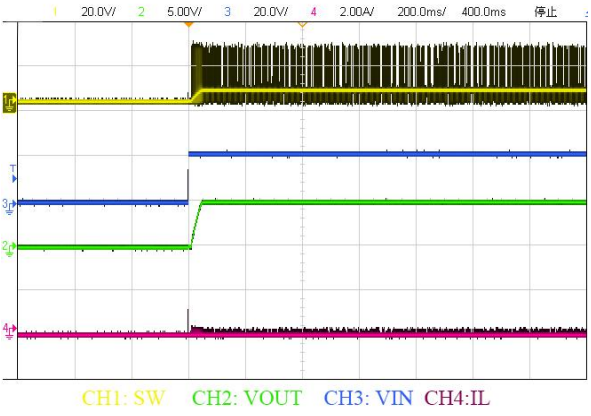
Vin = 12V, Vout = 5V

Fig. 9 Shutdown waveform, Iout = 0A



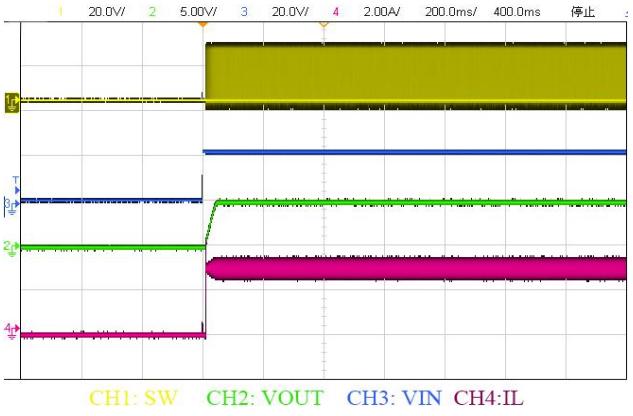
Vin = 12V, Vout = 5V

Fig. 10 Shutdown waveform, Iout = 3A



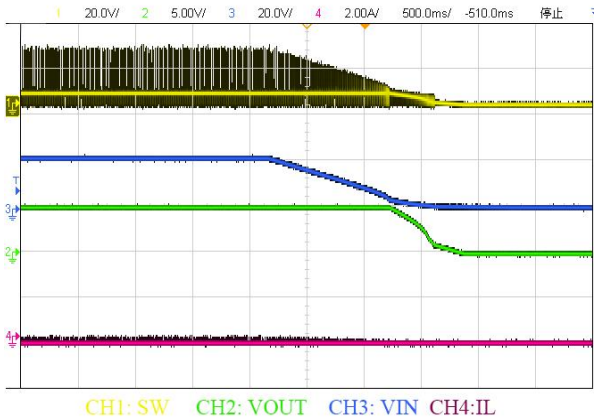
Vin = 24V, Vout = 5V

Fig. 11 Startup waveform, Iout = 0A



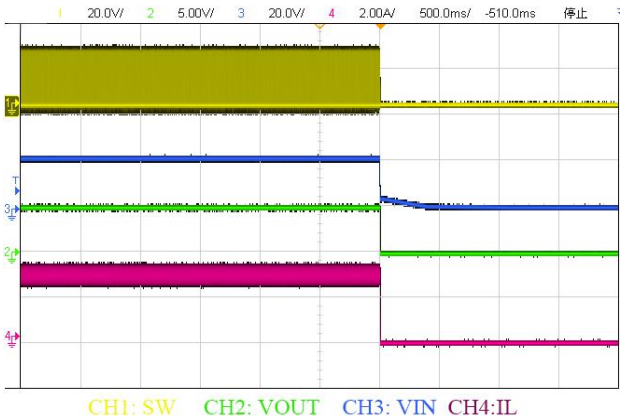
Vin = 24V, Vout = 5V

Fig. 12 Startup waveform, Iout = 3A



Vin = 24V, Vout = 5V

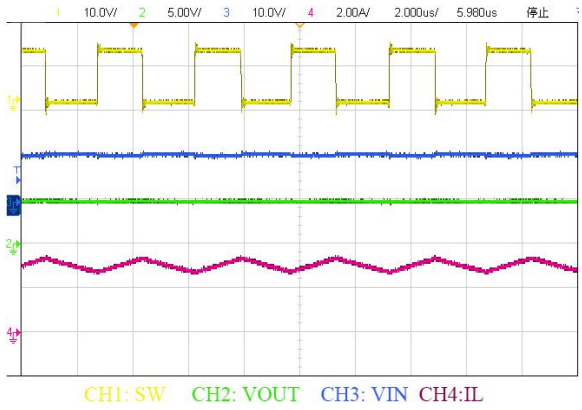
Fig. 13 Shut down waveform, Iout = 0A



Vin = 24V, Vout = 5V

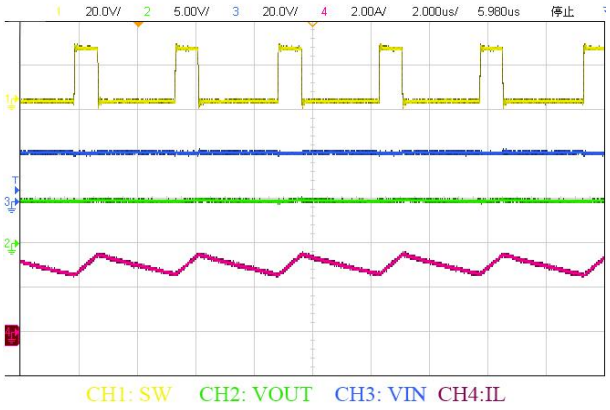
Fig. 14 Shutdown waveform, Iout = 3A

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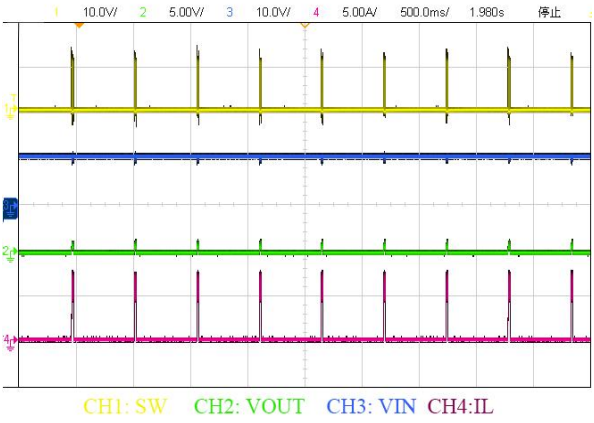
Vin = 12V, Vout = 5V

Fig. 15 Steady State, Iout = 3A



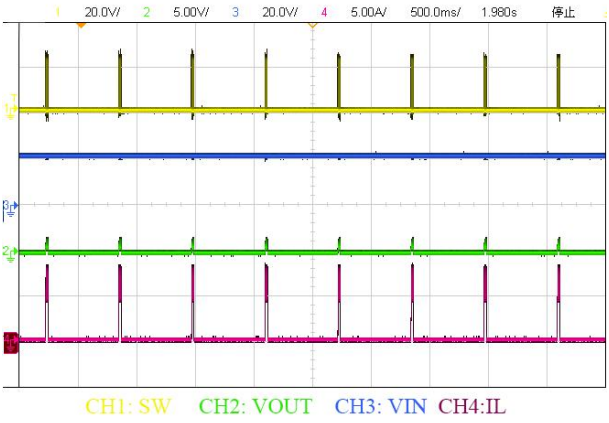
Vin = 24V, Vout = 5V

Fig. 16 Steady State, Iout = 3A



Vin = 12V, Vout = 5V

Fig. 17 Short Circuit waveform



Vin = 24V, Vout = 5V

Fig. 18 Short Circuit waveform

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9 Detailed Description

9.1 Overview

PL8332G is an easy to use synchronous step-down DC-DC converter that operates from 6.5V to 36V supply voltage. It is capable of delivering up to 3.1A continuous load current with high efficiency and thermal performance in a very small solution size.

PL8332G also integrates input over voltage and output over voltage protection. This feature helps customers to design a safe DC-DC converter easily.

The switching frequency is fixed at 300KHz to minimize inductor size and improve EMI performance. The soft-start time can be adjusted through SS pin capacitor.

9.2 Functional Block Diagram

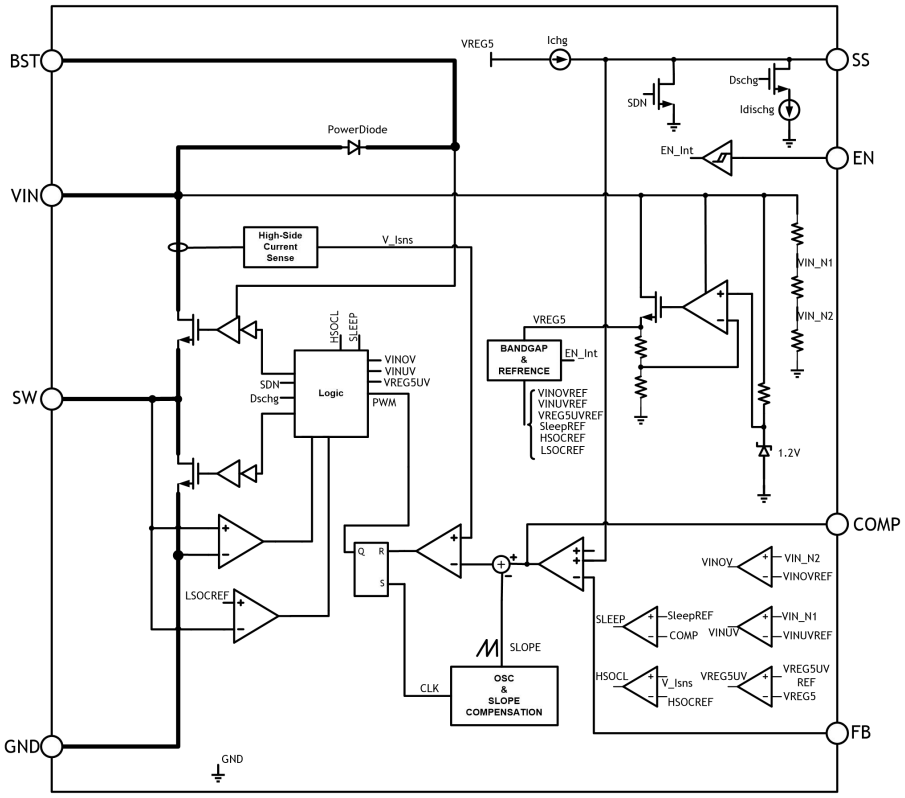


Fig.19 PL8332G Diagram

9.3 Peak Current Mode Control

PL8332G employs a fixed 300KHz frequency peak current mode control. The output voltage is sensed by an external feedback resistor string on FB pin and fed to an internal error amplifier. The output of error amplifier will compare with high side current sense signal by an internal PWM comparator. When the second signal is higher than the first one, the PWM comparator will generate a turn-off signal to turn off high side switch. The output voltage of error amplifier will increase or decrease proportionally with the output load current. PL8332G has a cycle-by-cycle peak current limit feature inside to help maintain load current in a safe region.

9.4 Sleep Operation for Light Load Efficiency

PL8332G has an internal feature to help improving light load efficiency. When output current is low, PL8332G will go into sleep mode.

9.5 Voltage Reference

Internal circuit produces a precise ±1.5% voltage reference over temperature supported by PL8332G.

9.6 Setting Output Voltage

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The output voltage is set with a resistor divider from the output node to the FB pin. 1% resistance accuracy of this resistor divider is preferred. The output voltage value is set as equation 1 below (R_1 is the upper resistor, R_2 is the lower resistor).

$$V_{out}=V_{ref}\times\frac{R_1+R_2}{R_2} \quad (1)$$

V_{ref} is the internal reference voltage of PL8332G, which is 0.9V.

9.7 Setting Enable Threshold

When the voltage at EN pin exceeds the threshold, PL8332G begins to work. When keeping EN low (below threshold), PL8332G stops working. The quiescent current of PL8332G is very low to maintain a good shut down operation for system.

PL8332G has an internal pull up resistor to make sure IC work when EN pin is float. If an application requires controlling EN pin, use open drain or open collector output logic circuit to interface with it. **It is strongly recommended to increase the Schottky diode from the SS pin to the EN pin.**

When system needs a higher VIN UVLO threshold, the EN pin can be configured as shown in Figure 20 below.

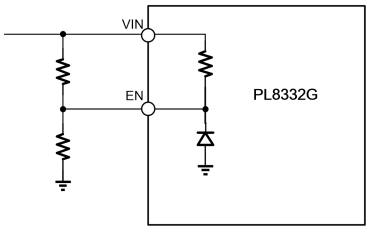


Fig.20 Adjustable VIN Voltage Lockout

9.8 Error Amplifier

PL8332G has a trans-conductance error amplifier. It compares FB voltage with the lower one between 0.9V reference voltage and the soft-start voltage appearing at SS pin. The frequency compensation components are placed at COMP pin.

9.9 Slope Compensation

In order to avoid sub-harmonic oscillation at high duty cycle, PL8332G adds a slope compensation ramp to the sensed signal of current flowing through high side switch.

9.10 Bootstrap Voltage provided by internal LDO

PL8332G has an internal LDO to provide energy consumed by high side switch. At BST pin, PL8332G needs a small ceramic capacitor like 100nF between BST and SW pin to provide gate-drive voltage for high side switch. The bootstrap capacitor is charged when high side is off. In Continuous-Current-Mode, the bootstrap capacitor will be charged when low side is on. The bootstrap capacitor voltage will be maintained at about 5.3V. When IC works under sleep mode, what value the bootstrap capacitor is charged depends on the difference of VIN and output voltage. However, when the voltage on the bootstrap capacitor is below bootstrap voltage refresh threshold, PL8332G will force low side on to charge bootstrap capacitor. Connecting an external diode from the output of regulator to the BST pin will also work and increase the efficiency of the regulator when output is high enough.

In order to improve EMI performance, a resistor can be connected between BST pin and bootstrap capacitor to slow down the turn-on speed of high side power switch.

9.11 Soft-Start and Hiccup

PL8332G needs a capacitor at SS pin to support soft-start function. The soft-start time can be adjusted by setting different soft-start capacitor at this pin. There is an internal 2.3uA current to charge SS capacitor when it starts to work. The capacitor is also used to configure the short circuit hiccup rest time. After soft-start period is ended, when V_{FB}<0.3V , PL8332G will go into hiccup mode to limit average load current. PL8332G will exit hiccup mode once the over current condition is removed.

9.12 High Side Over-Current Protection

In PL8332G, high-side MOSFET current is sensed. This sensed signal will compare the lower voltage between COMP pin voltage and over current threshold. High-side MOSFET will be turned off when the sensed current reaches the lower voltage. In normal operation, COMP pin voltage will be lower. If the over current threshold is lower, PL8332G enters over current protection mode.

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9.13 Over-Current Protection

When the low-side MOSFET is turned on, the conduction current is monitored and the SW voltage is sensed. When the difference between GND and SW is higher than an internal threshold, it means PL8332G is under over current mode. The high side switch won't be turned on until low side MOSFET's current is lower than the over current limit.

When the low side MOSFET current reaches zero, it will be immediately turned off to improve conversion efficiency.

9.14 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 155°C typically. When the junction temperature drops below 140°C, IC will start to work again.

10 Application and Implementation

10.1 Inductor selection

An inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 25% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s\times\Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum peak current. The peak inductor current can be calculated by:

$$I_{L_P}=I_{load}+\frac{V_{OUT}}{2\times f_s\times L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Where I_{load} is the load current.

The choice of inductor material mainly depends on the price vs. size requirements and EMI constraints.

10.2 Optional Schottky Diode

During the transition between the high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled with low side MOSFET to improve overall efficiency. Table 2 lists example Schottky diodes and their Manufacturers.

Table 2 – Diode Selection Guide

Part Number	Voltage/Current Rating	Vendor
SS25FA	50V/2A	Fairchild
B240A	40V/2A	Vishay

10.3 Input capacitors selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C_{IN}) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2\times V_{OUT}$, where:

$$I_{CIN}=\frac{I_{load}}{2} \quad (5)$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

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When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN}=\frac{I_{load}}{f_s\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

C_{IN} is the input capacitance.

10.4 Output capacitors selection

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended.

Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_s\times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor and C_{OUT} is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_s^{2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulator. PL8332G is optimized for a wide range of capacitance and ESR values.

10.5 External bootstrap diode

It is recommended that an external bootstrap diode could be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The bootstrap diode can be a low cost one such as IN4148 or BAT54.

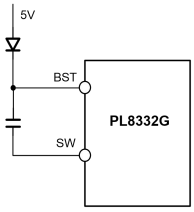


Fig.21External Bootstrap Diode

This diode is also recommended for high duty cycle operation (when (V_{OUT}/V_{IN}) > 65%) and high output voltage (V_{OUT}>12V) applications.

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11 PCB Layout

11.1 Guideline

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R_1 and R_2, should be kept close to FB pin. V_{out} sensing path should stay away from noisy nodes, such as SW and BST signals and preferably through a layer on the other side of shielding layer.
2. The input bypass capacitor C_1 and C_2 must be placed as close as possible to the V_{IN} pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the V_{IN} pin to reduce the high frequency injection current.
3. The inductor L1 should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor, C_3, and C_4 should be placed close to the junction of L1. The L1, C_3, and C_4 trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. The ground connection for C_1, C_2 and C_3, C_4 should be as small as possible and connect to system ground plane at only one spot (preferably at the C_3, C_4 ground point) to minimize injecting noise into system ground plane.

11.2 Example

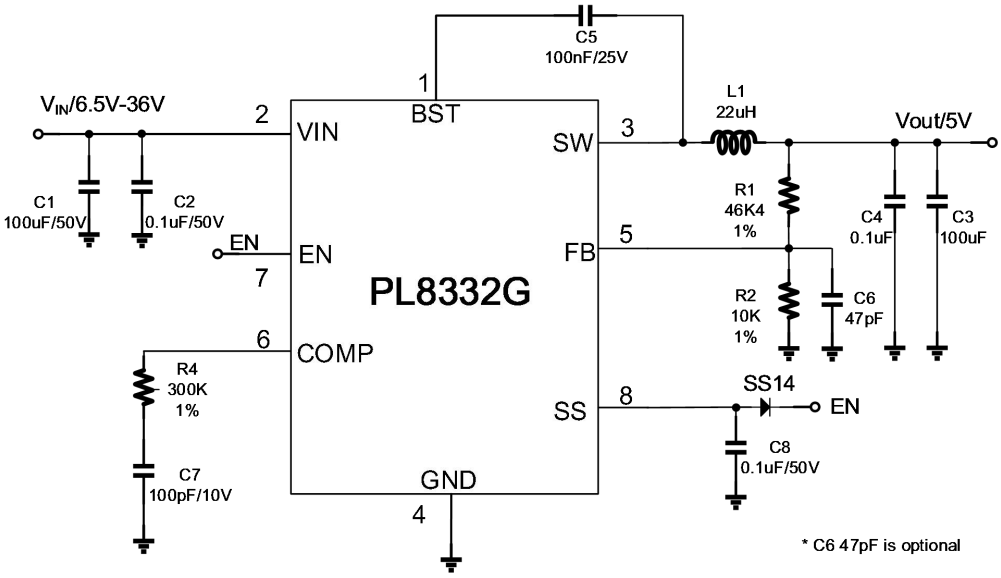


Fig.22 Schematic

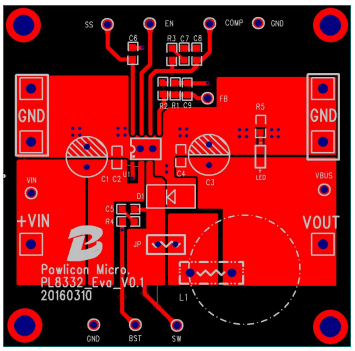


Fig. 23 Top layer layout

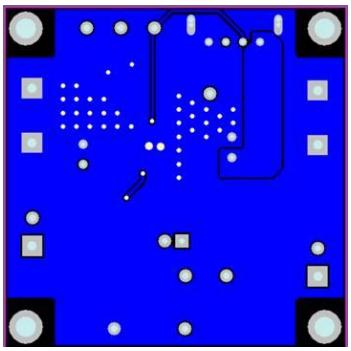
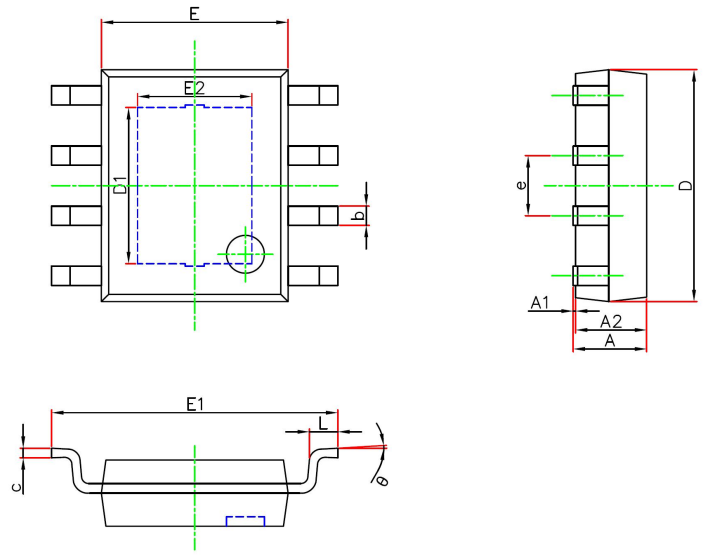


Fig. 24 Bottom layer layout

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12 Packaging Information

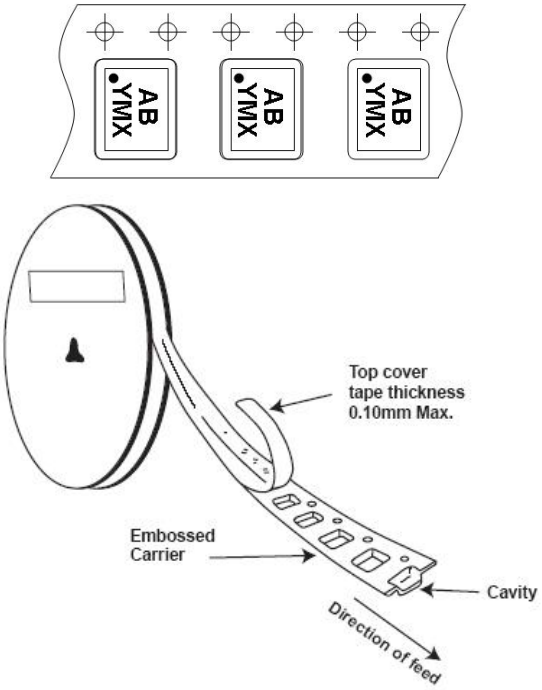
ESOP-8 (95x130) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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13 Taping Orientation



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