PL89021 100V, 1A Step-Down Converter With Ultra Low IQ

1 Features

- Wide input voltage range of 5V to 100V
- Junction temperature range: –40°C to +150°C
- Fixed 3ms internal soft start timer
- Peak and valley current limit protection
- EN UVLO and thermal shutdown protection
- Low minimum on and off times of 100ns/200ns
- Adjustable switching frequency up to 2MHz
- 5μA shutdown quiescent current CC
- COT mode control architecture
- Integrated high side 0.7Ω NFET and low side 0.34Ω NFET switch supports wide duty cycle range
- 1.2V internal voltage reference
- No loop compensation components
- Internal VCC bias regulator and boot diode
- Open drain power good indicator
- ESOP8 package

2 Applications

- Appliances, power and garden tools
- High-cell-count battery packs (E-Bike, E-Scooter)
- Motor drives, drones, telecom

3 Description

The PL89021 synchronous buck converter is designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components. A minimum controllable on time of 100ns facilitates large step down conversion ratios, enabling the direct step down from a 48V nominal input to low-voltage rails for reduced system complexity and solution cost.The PL89021 operates during input voltage dips as low as 5V, at nearly 100% duty cycle if needed, making it an excellent choice for wide input supply range industrial and high cell count battery pack applications.

With integrated high side and low side power MOSFETs, the PL89021 delivers up to 1A of output current. A constant on time (COT) control architecture provides nearly constant switching frequency with excellent load and line transient response. Additional features of the PL89021 include ultra low IQ and high light load efficiency, innovative peak and valley over current protection, integrated VCC bias supply and bootstrap diode, precision enable and input UVLO, and thermal shutdown protection with automatic recovery. An open drain PGOOD indicator provides sequencing, fault reporting, and output voltage monitoring.

4 Typical Application Schematic

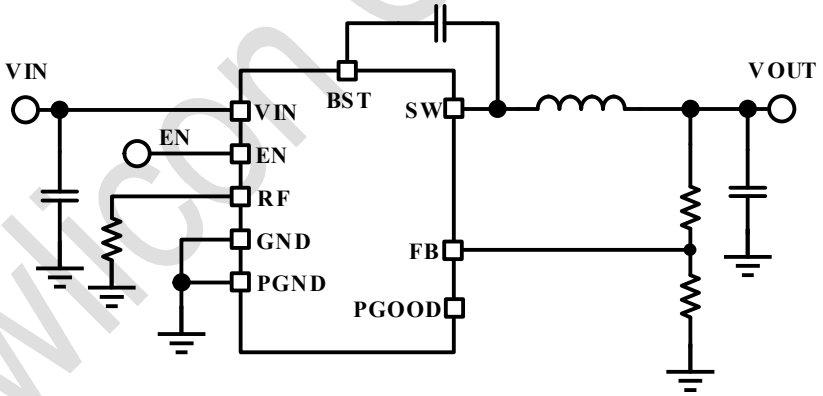


Fig. 4-1 Typical Application Schematic

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5 Pin Configuration and Functions

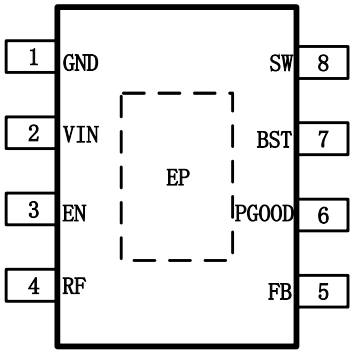


Fig. 5-1 Pin-Function

Pin		Description
Number	Name	
1	GND	Ground connection for internal circuits
2	VIN	Regulator supply input pin to high side power MOSFET and internal bias regulator. Connect directly to the input supply of the buck converter with short, low impedance paths.
3	EN/UVLO	Precision enable and under voltage lockout (UVLO) programming pin. If the EN/UVLO voltage is below 1.1V, the converter is in the shutdown mode with all functions disabled. If the UVLO voltage is greater than 1.1V and below 1.5V, the converter is in standby mode with the internal VCC regulator operational and no switching. If the EN/UVLO voltage is above 1.5V, the start up sequence begins.
4	RF	On time programming pin. A resistor between this pin and GND sets the buck switch on time.
5	FB	Feedback input of voltage regulation comparator.
6	PGOOD	Power good indicator. This pin is an open drain output pin. Connect to a source voltage through an external pull up resistor between 10kΩ to 100kΩ
7	BST	Bootstrap gate drive supply.
8	SW	Switching node that is internally connected to the source of the high side NMOS buck switch and the drain of the low side NMOS synchronous rectifier. Connect to the switching node of the power inductor.
9	EP	Exposed pad of the package. No internal electrical connection. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

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6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL89021	PL89021IES08A	ESOP8	4000	89021 RAAYMD

89021: Part Number
RAAYMD : RAA: LOT NO.; YMD: Package Date Code

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7 Specifications

7.1 Absolute Maximum Ratings(Note1)

PARAMETER	MIN	MAX	Unit
VIN to GND	-0.3	100	V
EN to GND	-0.3	100	
FB to GND	-0.3	5.5	
RF to GND	-0.3	5.5	
BST to GND	-0.3	105.5	
BST to SW	-0.3	5.5	
SW to GND	-1.5	100	
PGOOD to GND	-0.3	100	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature	-40	+150	°C
V_{ESD}	HBM Human body model	2		kV

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	VIN	5.0	100	V
Temperature	Operating junction temperature range, T_J	-40	+150	°C

7.4 Thermal Information(Note 3)

Symbol	Description	ESOP8	Unit
θ_{JA}	Junction to ambient thermal resistance	41.1	°C/W
θ_{JC}	Junction to case thermal resistance	37.3	
θ_{JB}	Junction to board thermal resistance	30.6	

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

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7.5 Electrical Characteristics

Typical values correspond to TJ = 25°C. Minimum and maximum limits apply over the full –40°C to 150°C junction temperature range unless otherwise indicated. VIN = 36 V and VEN/UVLO = 2 V unless otherwise stated.

Supply voltages	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$I_{Q-SHUTDOWN}$	VIN shutdown current	V_{EN} = 0 V		2.5	5	uA
$I_{Q-ACTIVE}$	VIN active current	V_{EN} = 2.5 V	15	25	50	uA
UVLO/EN						
$V_{SD-RISING}$	Shutdown threshold	V_{EN} rising			1.1	V
$V_{SD-FALLING}$	Shutdown threshold	V_{EN} falling	0.45			V
$V_{EN-RISING}$	Enable threshold	V_{EN} rising	1.45	1.5	1.55	V
$V_{EN-FALLING}$	Enable threshold	V_{EN} falling	1.35	1.4	1.44	V
FEEDBACK						
V_{REF}	FB regulation voltage	V_{FB} falling	1.18	1.2	1.218	V
FREQUNEC						
Freq1		R_{RF}=200kΩ		500		kHz
Freq2		R_{RF}=330kΩ		300		kHz
Freq3		R_{RF}=500kΩ		200		kHz
PGOOD						
V_{PG-UTH}	FB upper threshold for PGOOD high to low	V_{FB} rising	1.105	1.14	1.175	V
V_{PG-LTH}	FB lower threshold for PGOOD high to low	V_{FB} falling	1.055	1.08	1.1	V
V_{PG-HYS}	PGOOD upper and lower threshold hysteresis	V_{FB} falling		60		mV
R_{PG}	PGOOD pull down resistance	V_{FB} = 1 V		200		Ω
BOOTSTRAP						
V_{BST-UV}	Gate drive UVLO	V_{BST} rising		2.7	3.4	V
POWER SWITCHES						
$R_{DSON-HS}$	High-side MOSFET RDSON	I_{SW} = –100 mA		0.7		Ω
$R_{DSON-LS}$	Low-side MOSFET RDSON	I_{SW} = –100 mA		0.34		Ω
SOFT START						
t_{SS}	Internal soft-start time		3			ms
CURRENT LIMIT						
I_{PEAK}	Peak current limit threshold (HS)		1.2			A
THERMAL SHUTDOWN						
TSD	Thermal shutdown threshold	TJ rising		175		°C
TSD-HYS	Thermal shutdown hysteresis			10		°C

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8 Typical Characteristics

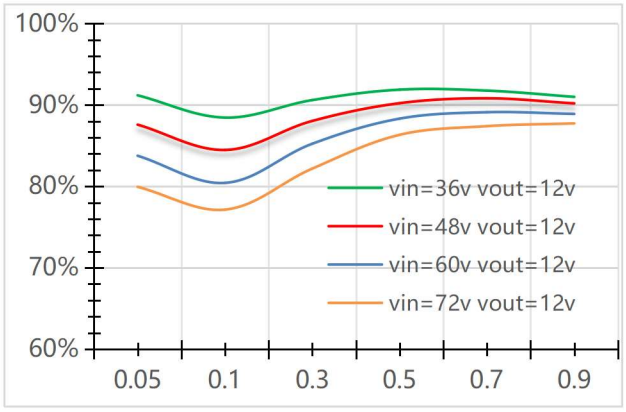


Fig.8-1 Efficiency

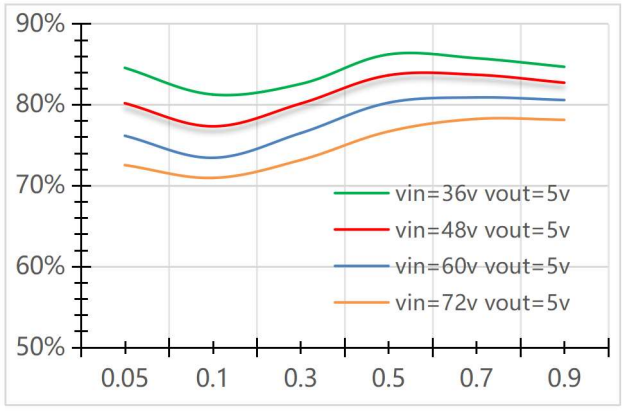
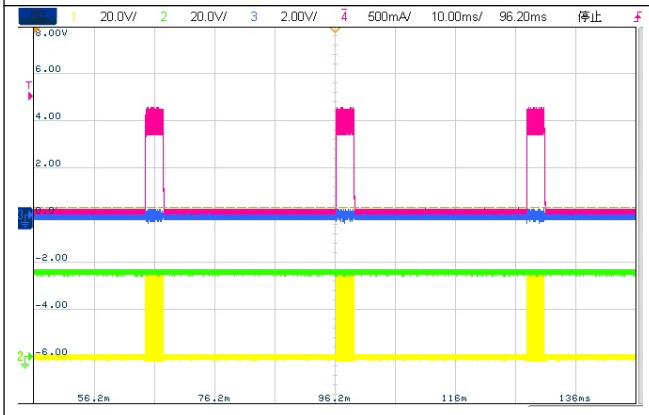


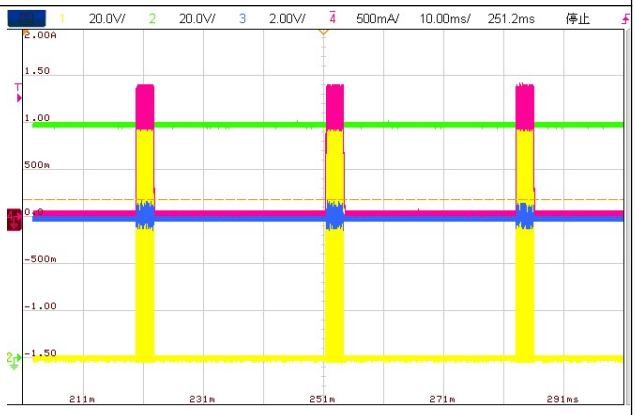
Fig.8-2 Efficiency



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=36V Vout=12V

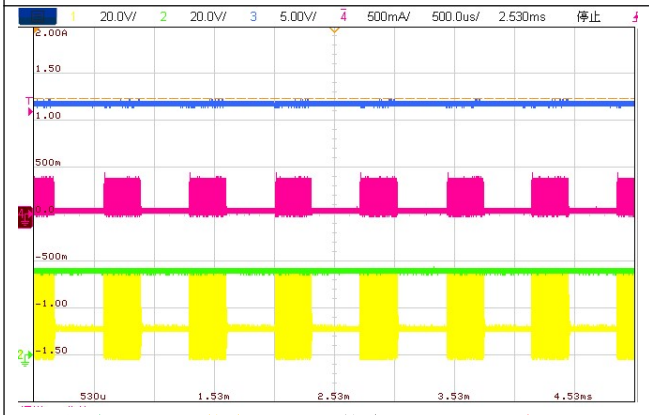
Fig.8-3 Short Circuit waveform



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=100V Vout=12V

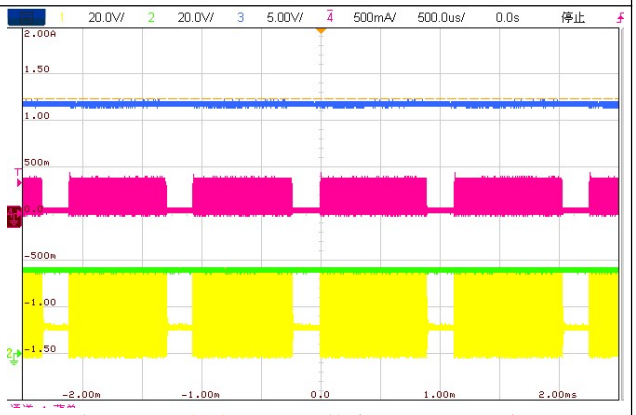
Fig.8-4 Short Circuit waveform



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=36V Vout=12V

Fig.8-5 Steady State waveform, Iout =0.05A

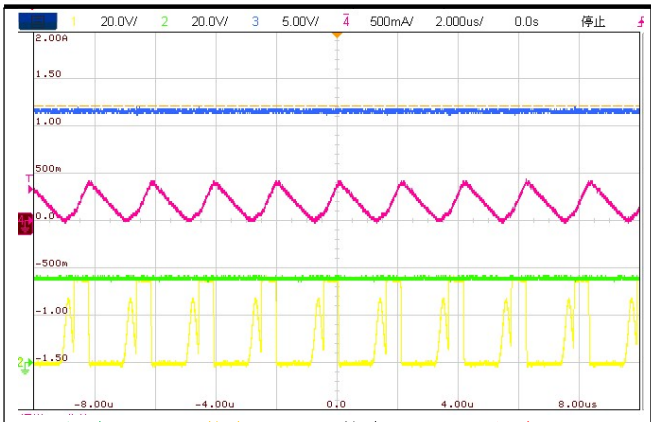


绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=36V Vout=12V

Fig.8-6 Steady State waveform, Iout =0.1A

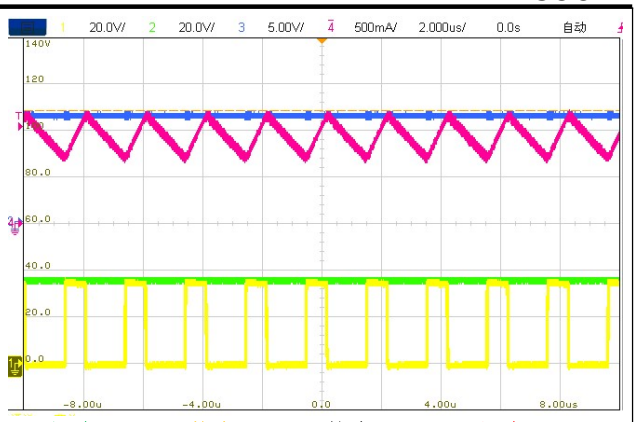
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绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=36V Vout=12V

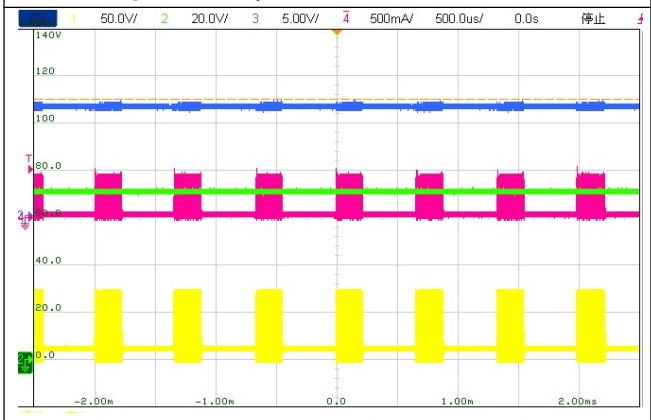
Fig.8-7 Steady State waveform, Iout =0.15A



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Vin=36V Vout=12V

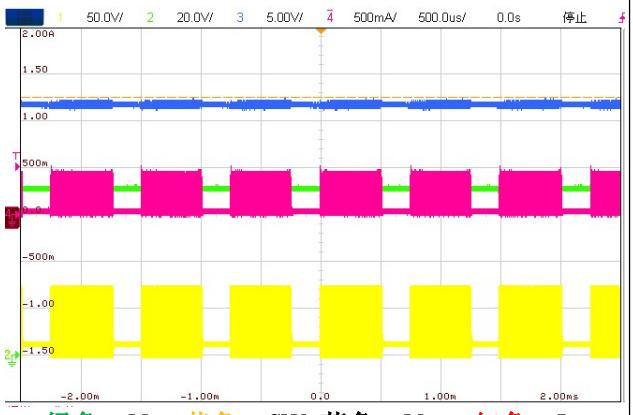
Fig.8-8 Steady State waveform, Iout =0.9A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=72V Vout=12V

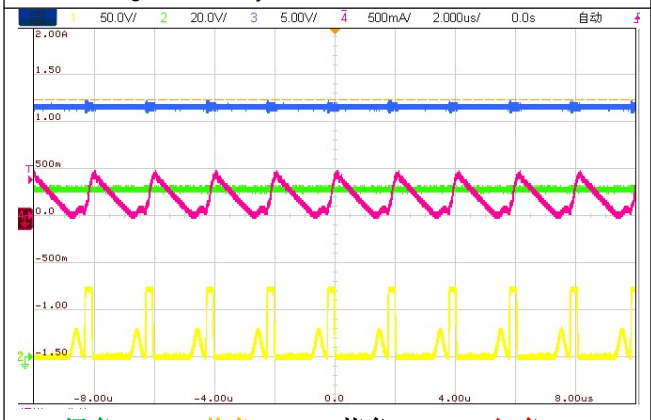
Fig.8-9 Steady State waveform, Iout =0.05A



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Vin=72V Vout=12V

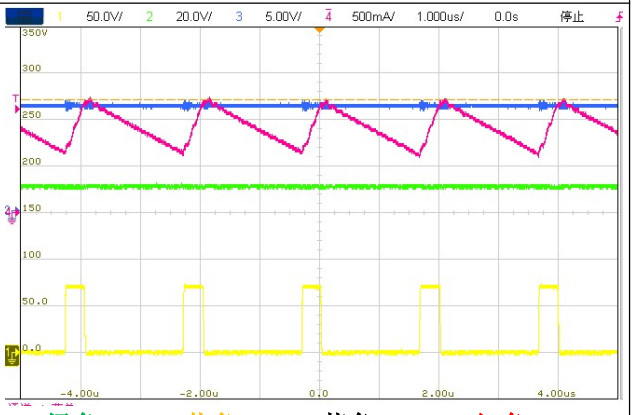
Fig.8-10 Steady State waveform, Iout =0.1A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=72V Vout=12V

Fig.8-11 Steady State waveform, Iout =0.16A

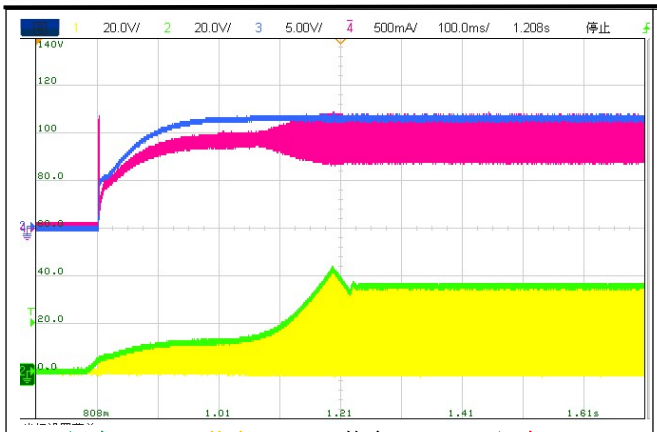


绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=72V Vout=12V

Fig.8-12 Steady State waveform, Iout =0.9A

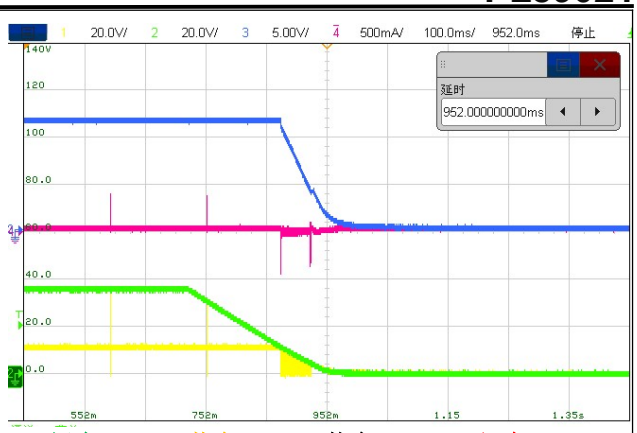
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绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=36V Vout=12V

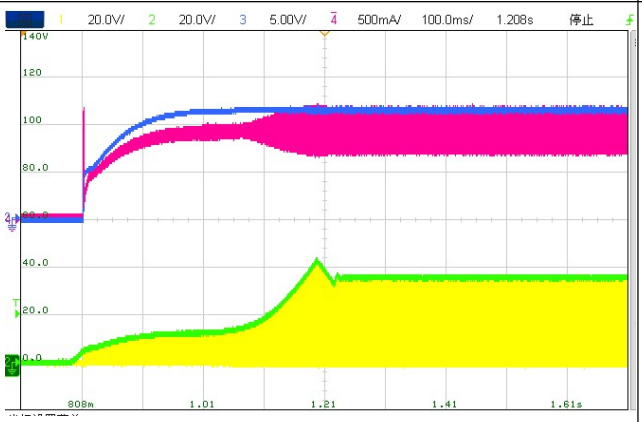
Fig.8-13 Vin Start up waveform, Iout =0A



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Vin=36V Vout=12V

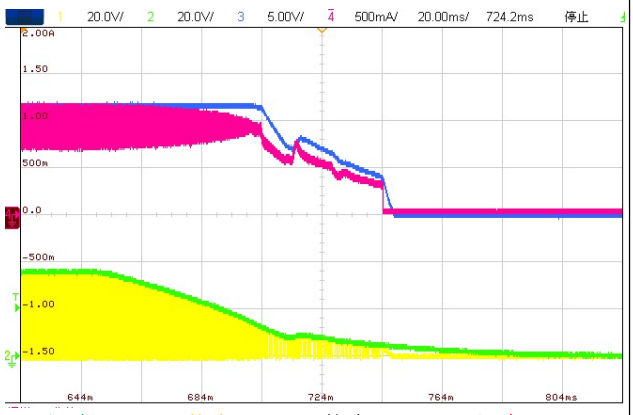
Fig.8-14 Vin Shut down waveform, Iout =0A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=36V Vout=12V

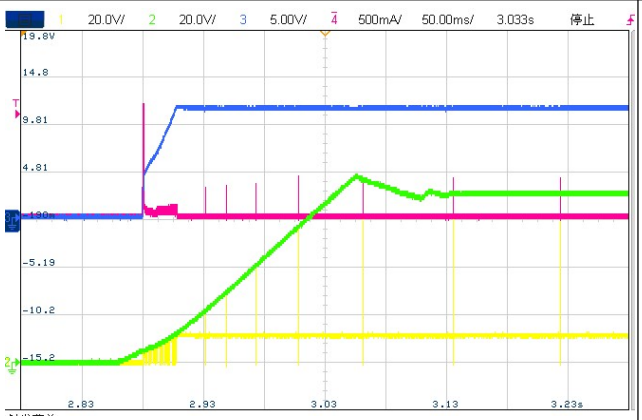
Fig.8-15 Vin Start up waveform, Iout =0.9A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=36V Vout=12V

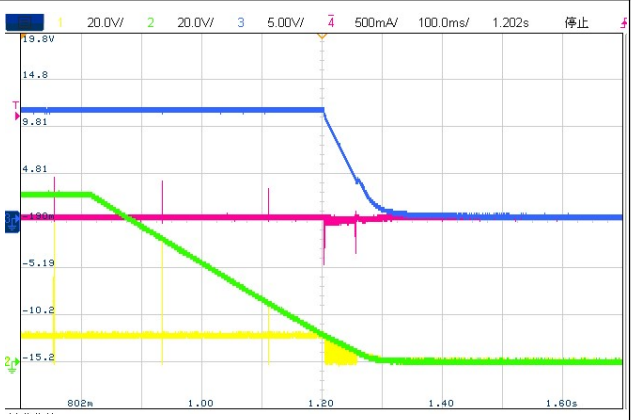
Fig.8-16 Vin Shut down waveform, Iout =0.9A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=72V Vout=12V

Fig.8-17 Vin Start up waveform, Iout =0A

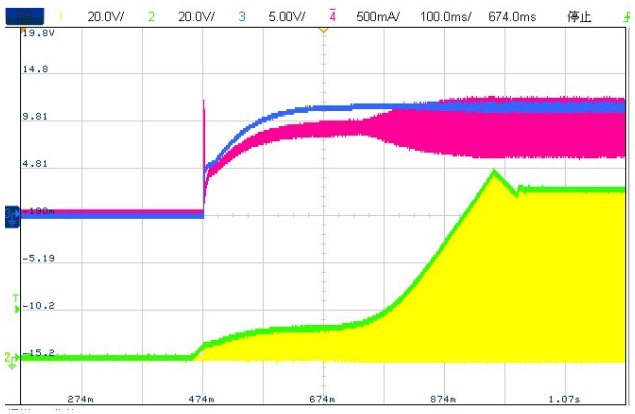


绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=72V Vout=12V

Fig.8-18 Vin Shut down waveform, Iout =0A

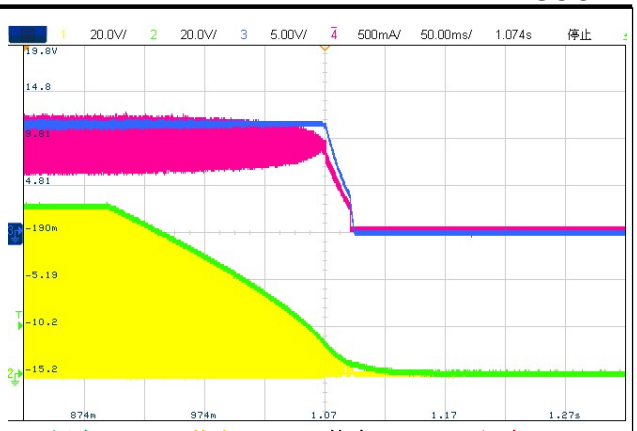
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绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=72V Vout=12V

Fig.8-19 Vin Start up waveform, Iout =0.9A



绿色：Vin 黄色：SW 蓝色：Vout 红色：IL

Vin=72V Vout=12V

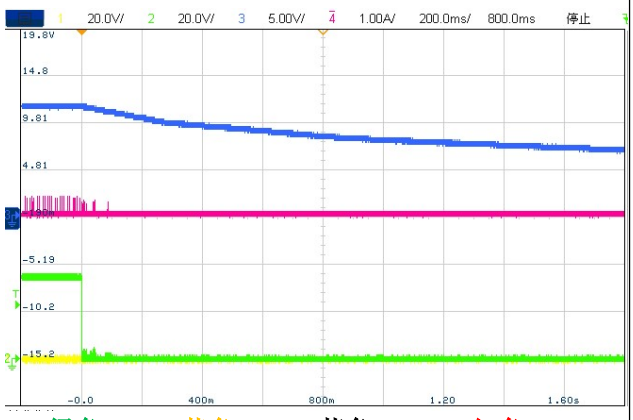
Fig.8-20 Vin Shut down waveform, Iout =0.9A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=36V Vout=12V

Fig.8-21 EN Start up waveform, Iout =0A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=36V Vout=12V

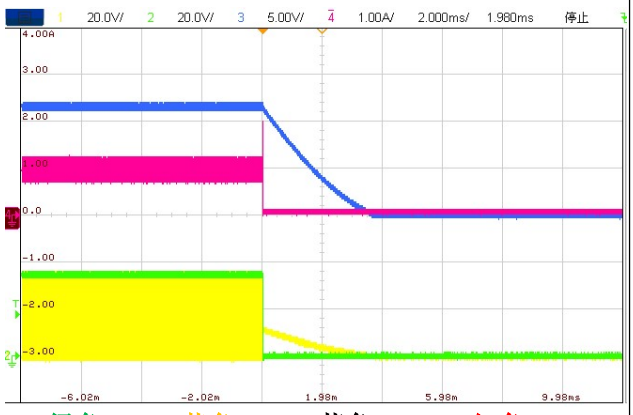
Fig.8-22 EN Shut down waveform, Iout =0A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=36V Vout=12V

Fig.8-23 EN Start up waveform, Iout =0.9A

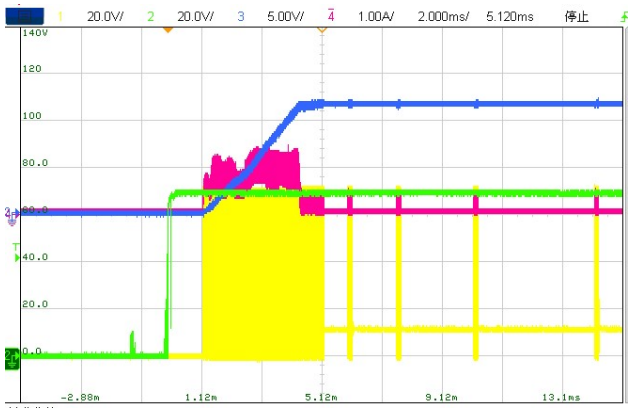


绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=36V Vout=12V

Fig.8-24 EN Shut down waveform, Iout =0.9A

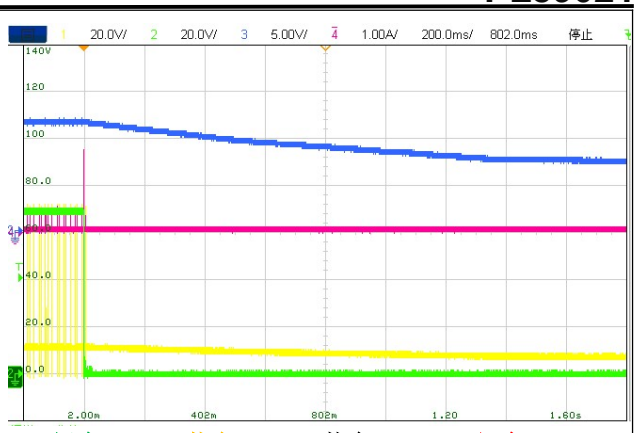
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绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=72V Vout=12V

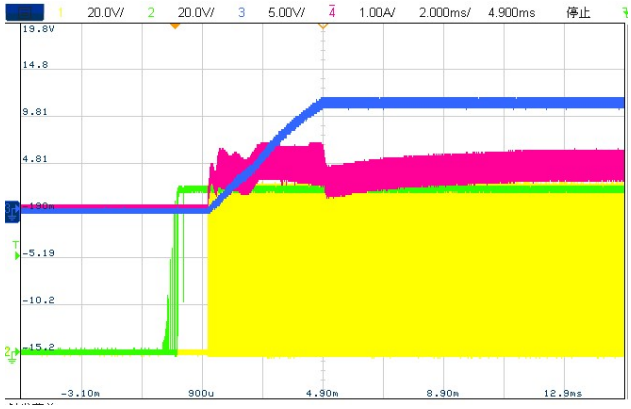
Fig.8-25 EN Start up waveform, Iout =0A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=72V Vout=12V

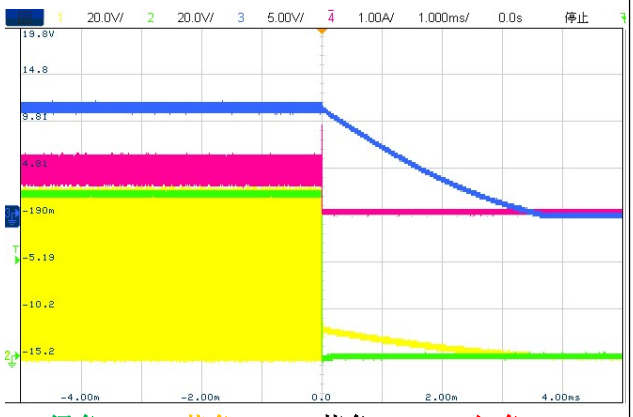
Fig.8-26 EN Shut down waveform, Iout =0A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=72V Vout=12V

Fig.8-27 EN Start up waveform, Iout =0A



绿色：EN 黄色：SW 蓝色：Vout 红色：IL

Vin=72V Vout=12V

Fig.8-28 EN Shut down waveform, Iout =0A

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9 Detailed Descriptions

9.1 Overview

The PL89021 is an easy to use, ultra low IQ constant on time (COT) synchronous step down buck regulator. With integrated high side and low side power MOSFETs, the PL89021 is a low cost, highly efficient buck converter that operates from a wide input voltage of 5V to 100V, delivering up to 1A DC load current. The PL89021 is available in the ESOP8 package. This constant on time (COT) converter is ideal for low noise, high current, and fast load transient requirements, operating with a predictive on time switching pulse. Over the input voltage range, input voltage feed forward is employed to achieve a quasi fixed switching frequency. A controllable on time as low as 100ns permits high step down ratios and a minimum forced off time of 200ns provides extremely high duty cycles allowing VIN to drop close to VOUT before frequency fold back occurs. At light loads the device transitions into an ultra low IQ mode to maintain high efficiency and prevent draining battery cells connected to the input when the system is in standby. The PL89021 implements a smart peak and valley current limit detection circuit to ensure robust protection during output short circuit conditions. Control loop compensation is not required for this regulator, reducing design time and external component count. The PL89021 incorporates additional features for comprehensive system requirements, including an open drain Power Good circuit for power rail sequencing and fault reporting, internally fixed soft start, monotonic start up into prebiased loads, smart cycle by cycle current limit for optimal inductor sizing, and thermal shutdown with automatic recovery. These features enable a flexible and easy to use platform for a wide range of applications. The PL89021 supports a wide range of endequipment systems requiring a regulated output from a high input supply where the transient voltage deviates from its DC level. Examples of such end equipment systems are 48V automotive systems, high cell count battery pack systems, 24V industrial systems, and 48V telecom and PoE voltage ranges. The pin arrangement is designed for a simple layout requiring only a few external components.

9.2 Functional Block Diagram

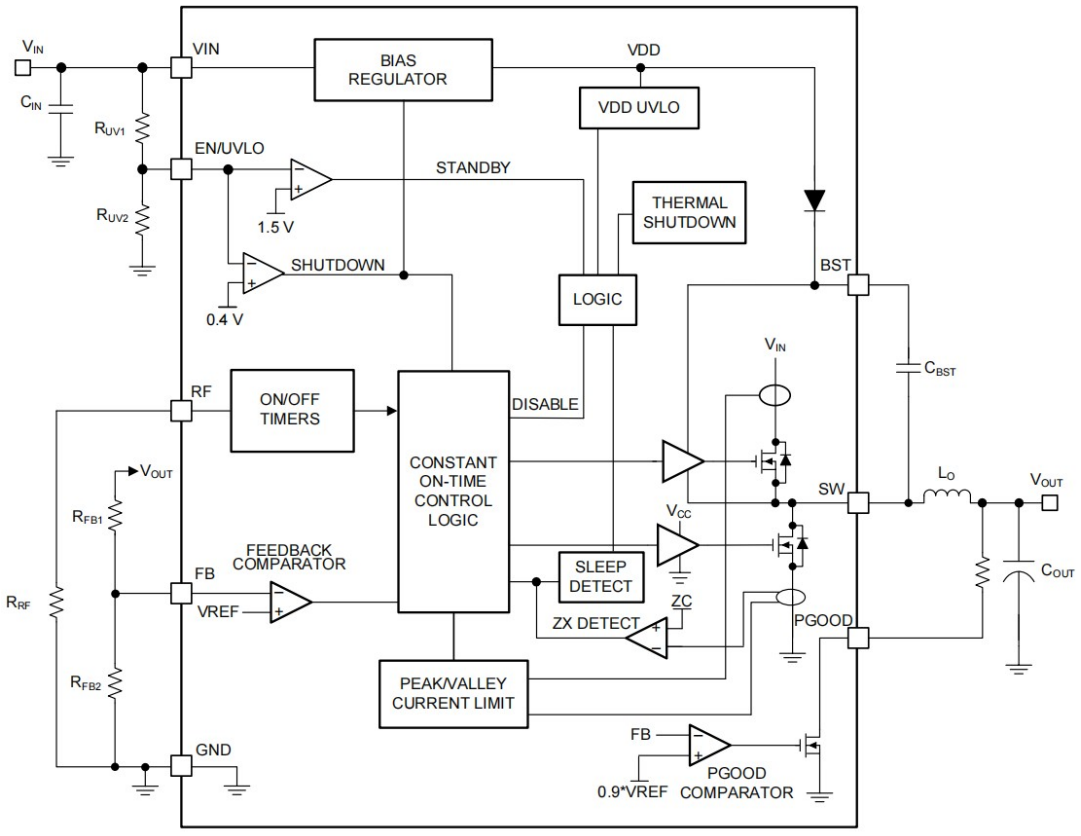


Fig. 9-2 Block Diagram

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9.3 Control Architecture

The PL89021 step down switching converter employs a constant on time (COT) control scheme. The COT control scheme sets a fixed on time t_{ON} of the high side FET using a timing resistor (RON). The t_{ON} is adjusted as Vin changes and is inversely proportion to input voltage to maintain a fixed frequency when in continuous conduction mode (CCM). After expiration of t_{ON}, the high side FET remains off until the feedback pin is equal or below the reference voltage of 1.2V. In order to maintain stability, the feedback comparator requires a minimal ripple voltage that is in phase with the inductor current during the off time. Furthermore, this change in feedback voltage during the off time must be large enough to dominate any noise present at the feedback node. The minimum recommended ripple voltage is 20mV. Refer to ***Table 9-3-1*** for different types of ripple injection schemes that ensure stability over the full input voltage range. During a rapid start up or a positive load step, the regulator operates with minimum off times until regulation is achieved. This feature enables extremely fast load transient response with minimum output voltage undershoot. When regulating the output in steady state operation, the off time automatically adjusts itself to produce the SW pin duty cycle required for output voltage regulation to maintain a fixed switching frequency.

Table 9-3-1. Ripple Generation Methods

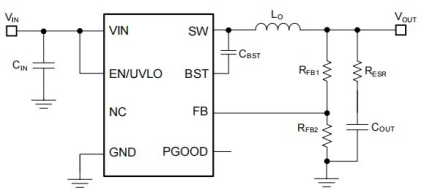
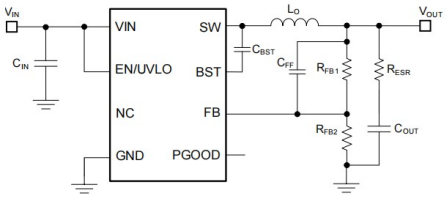
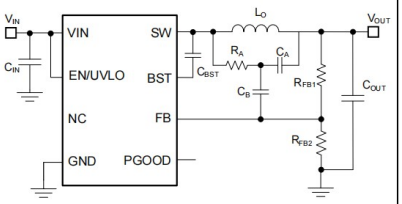
TYPE 1	TYPE 2	TYPE 3
Lowest Cost	Reduced Ripple	Minimum Ripple
		
$R_{ESR} \geq \frac{20mV \cdot V_{OUT}}{V_{FB1} \cdot \Delta I_{L(nom)}}$ (1) $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$ (2)	$R_{ESR} \geq \frac{20mV}{\Delta I_{L(nom)}}$ (3) $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$ (4) $C_{FF} \geq \frac{1}{2\pi \cdot F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$ (5)	$C_A \geq \frac{10}{F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$ (6) $R_A C_A \leq \frac{(V_{IN\text{-}nom} - V_{OUT}) \cdot t_{ON\ (@V_{IN\text{-}nom})}}{20mV}$ (7) $C_B \geq \frac{t_{TR\text{-}settling}}{3 \cdot R_{FB1}}$ (8)

Table 9-3-1 presents 3 different methods for generating appropriate voltage ripple at the feedback node. Type-1 ripple generation method uses a single resistor, R_{ESR} in series with the output capacitor. The generated voltage ripple has two components, capacitive ripple caused by the inductor ripple current charging and discharging the output capacitor and resistive ripple caused by the inductor ripple current flowing into the output capacitor and through series resistance R_{ESR}. The capacitive ripple component is out of phase with the inductor current and does not decrease monotonically during the off time. The resistive ripple component is in phase with the inductor current and decreases monotonically during the off time. The resistive ripple must exceed the capacitive ripple at VOUT for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters, with multiple on time bursts in close succession followed by a long off time. ***Equation 1*** and ***Equation 2*** define the value of the series resistance R_{ESR} to ensure sufficient in phase ripple at the feedback node.

Type-2 ripple generation uses a C_{FF} capacitor in addition to the series resistor. As the output voltage ripple is directly AC coupled by C_{FF} to the feedback node, the R_{ESR} and ultimately the output voltage ripple are reduced by a factor of V_{OUT} / V_{FB1}.

Type-3 ripple generation uses an RC network consisting of R_A and C_A, and the switch node voltage to generate a triangular ramp that is in phase with the inductor current. This triangular wave is the AC coupled into the feedback node with capacitor C_B. Because this circuit does not use output voltage ripple, it is suited for applications where low output voltage ripple is critical.

9.4 Internal VCC Regulator and Bootstrap Capacitor

The PL89021 contains an internal linear regulator that is powered from VIN with a nominal output of 5V, eliminating the need for an external capacitor to stabilize the linear regulator. The internal VCC regulator supplies current to internal circuit blocks including FET driver and logic circuits. The input pin (VIN) can be connected directly to line voltages up to 100V. As the power MOSFET has a low total gate charge, use a low bootstrap capacitor value to reduce the stress on the internal regulator. It is required to select a high quality 10~100nF 50V X7R ceramic bootstrap capacitor as specified in the Absolute Maximum Ratings. Selecting a higher value capacitance stresses the internal VCC regulator and damages the device. A lower capacitance than required may not be sufficient to drive the internal gate of the power MOSFET. An internal diode connects from the linear regulator to the BST pin to replenish the charge in the high side gate drive bootstrap capacitor when the SW voltage is low.

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9.5 Regulation Comparator

The feedback voltage at FB is compared to an internal 1.2V reference. The PL89021 voltage regulation loop regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage, V_{REF}. A resistor divider programs the ratio from output voltage V_{OUT} to FB. For a target V_{OUT} set point, calculate R_{FB2} based on the selected R_{FB1} using ***Equation 9.***

$$R_{FB2} = \frac{1.2V}{V_{OUT}-1.2V} \times R_{FB1} \quad (9)$$

Recommending selecting R_{FB1} in the range of 100kΩ to 1MΩ for most applications. A larger R_{FB1} consumes less DC current, which is mandatory if light load efficiency is critical. R_{FB1} larger than 1MΩ is not recommended as the feedback path becomes more susceptible to noise. It is important to route the feedback trace away from the noisy area of the PCB and keep the feedback resistors close to the FB pin.

9.6 Internal Soft Start

The PL89021 employs an internal soft start control ramp that allows the output voltage to gradually reach a steady state operating point, thereby reducing start up stresses and current surges. The soft start feature produces a controlled, monotonic output voltage start up. The soft start time is internally set to 3ms.

9.7 Adjustable Switching Frequency

Determine the R_{RF} resistor using ***Equation 10*** to set a specific switching frequency in CCM.

$$F_{SW}(kHz) = \frac{100000}{R_{RF}(k\Omega)} \quad (10)$$

9.8 Enable/Under voltage Lockout (EN/UVLO)

The PL89021 contains a dual level EN/UVLO circuit. When the EN/UVLO voltage is below 1.1V (typical), the converter is in a low current shutdown mode and the input quiescent current (IQ) is dropped down to 5μA. When the voltage is greater than 1.1V but less than 1.5V (typical), the converter is in standby mode. In standby mode the internal bias regulator is active while the control circuit is disabled. When the voltage exceeds the rising threshold of 1.5V (typical), normal operation begins. Install a resistor divider from VIN to GND to set the minimum operating voltage of the regulator.

9.9 Power Good (PGOOD)

The PL89021 provides a PGOOD flag pin to indicate when the output voltage is within the regulation level. Use the PGOOD signal for start up sequencing of downstream converters or for fault protection and output monitoring. PGOOD is an open drain output that requires a pull up resistor to a DC supply. The typical range of pull up resistance is10kΩ to 100kΩ. When the FB voltage exceeds 95% of the internal reference V_{REF}, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pull up. If the FB voltage falls below 90% of V_{REF}, an internal 25Ω PGOOD switch turns on and PGOOD is pulled low to indicate that the output voltage is out of regulation. The rising edge of PGOOD has a built in deglitch delay of 5μs.

9.10 Thermal Protection

The PL89021 includes an internal junction temperature monitor to protect the device in the event of a higher than normal junction temperature. If the junction temperature exceeds 175°C (typical), thermal shutdown occurs to prevent further power dissipation and temperature rise. The PL89021 initiates a restart sequence when the junction temperature falls to 165°C, based on a typical thermal shutdown hysteresis of 10°C. This is a nonlatching protection, and, as such, the device cycles into and out of thermal shutdown if the fault persists.

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10 Applications and Implementation

10.1 Selecting the Inductor

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current.

For a given ripple, the inductance terms in continuous mode are as ***Equation 11.***

$$L=\frac{V_{OUT}}{f_s\times\Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

where: f_s is operating frequency, kHz

ΔI_L is maximum inductor ripple current, A, usually select 20~40% maximum output current.

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

10.2 Output Capacitor (C_{OUT})

Select a ceramic output capacitor to limit the capacitive voltage ripple at the converter output. This is the sinusoidal ripple voltage that is generated from the triangular inductor current ripple flowing into and out of the capacitor. Select an output capacitance using ***Equation12*** to limit the voltage ripple component to 0.5% of the output voltage.

$$C_{OUT}\geq\frac{\Delta I_L}{8\times F_{SW}\times V_{OUT(ripple)}} \quad (12)$$

Substituting $\Delta I_{L(nom)}$ of 447mA gives C_{OUT} greater than 3.1μF. With voltage coefficients of ceramic capacitors taken in consideration, a 22μF, 25V rated capacitor with X7R dielectric is selected.

10.3 Input Capacitor (C_{IN})

An input capacitor is necessary to limit the input ripple voltage while providing AC current to the buck power stage at every switching cycle. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the VIN and GND pins of the PL89021. The input capacitors conduct a square wave current of peak to peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR related ripple component, the peak-to-peak ripple voltage amplitude is given by ***Equation13***.

$$V_{IN(ripple)}=\frac{I_{OUT}\times D\times(1-D)}{F_{SW}\times C_{IN}}+I_{OUT}\times R_{ESR} \quad (13)$$

The input capacitance required for a load current, based on an input voltage ripple specification (ΔVIN), is given by ***Equation14***:

$$C_{IN}\geq\frac{I_{OUT}\times D\times(1-D)}{F_{SW}\times(V_{IN(ripple)}-I_{OUT}\times R_{ESR})} \quad (14)$$

The recommended high-frequency input capacitance is 2.2μF or higher. Ensure the input capacitor is a high quality X7S or X7R ceramic capacitor with sufficient voltage rating for C_{IN}. Based on the voltage coefficient of ceramic capacitors, choose a voltage rating of twice the maximum input voltage. Additionally, some bulk capacitance is required if the PL89021 is not located within approximately 5cm from the input voltage source. This capacitor provides parallel damping to the resonance associated with parasitic inductance of the supply lines and high Q ceramics.

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11 PCB Layout

11.1 Guideline

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Place the input decoupling capacitor, catch diode, and the PL89021 (VIN, SW, and GND) as close to each other as possible.
2. Keep the power traces very short and fairly wide, especially for the SW node. This can help greatly reduce voltage spikes on the SW node and lower the EMI noise level.
3. Run the feedback trace as far from the inductor and noisy power traces (like the SW node) as possible.
4. Place thermal vias with 15mil barrel diameter and 40mil pitch (distance between the centers) under the exposed pad to improve thermal conduction.

11.2 Application Examples

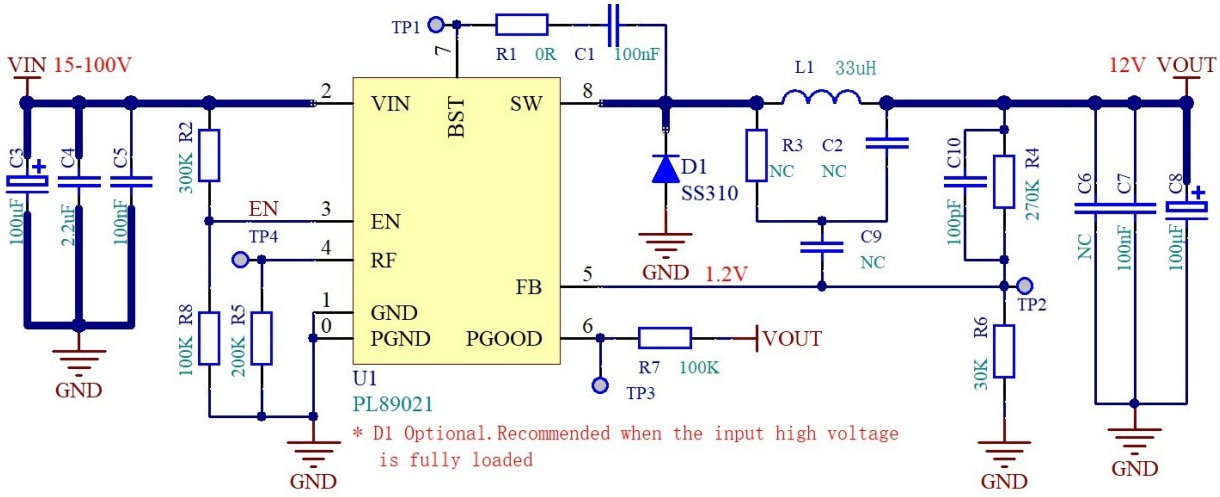


Fig. 11-2-1 Schematic

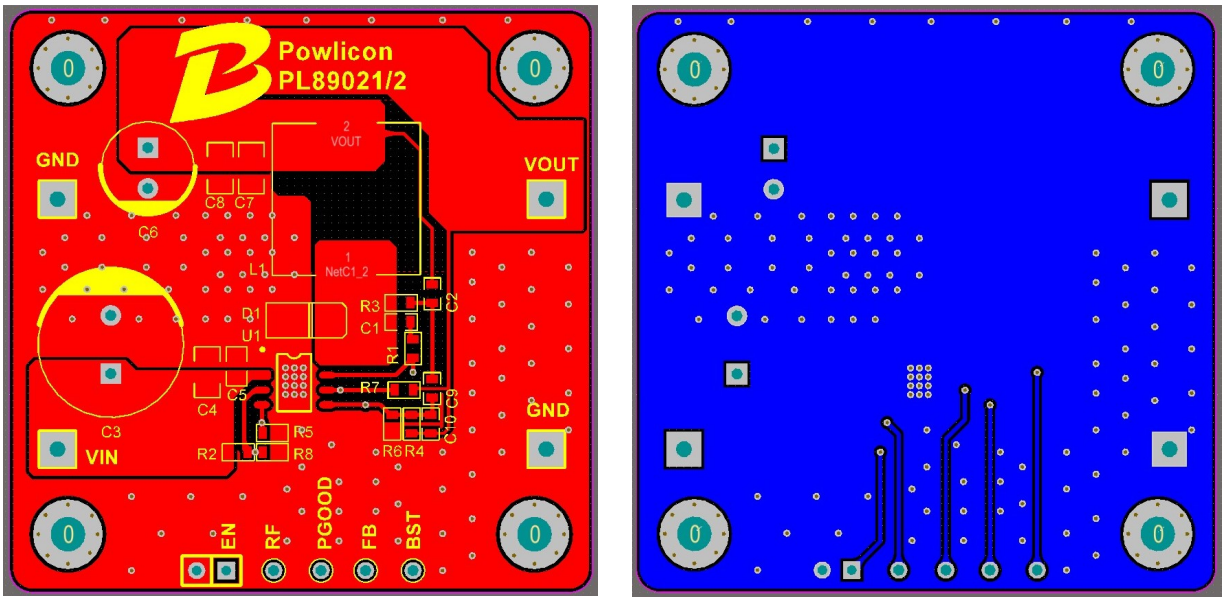
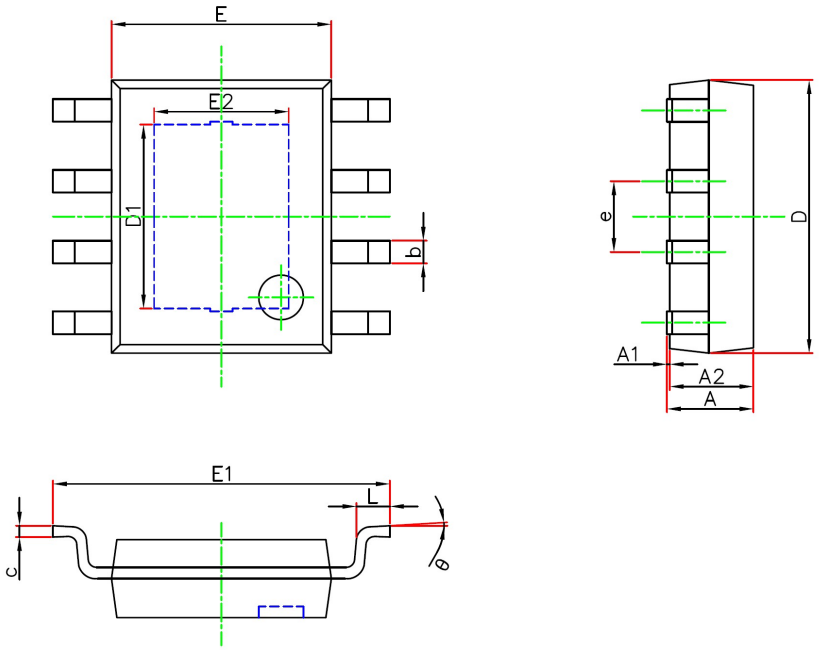


Fig. 11-2-3 PCB

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12 Packaging Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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