100V, Synchronous PWM Buck Controller

1 Features

- 12V to 100V wide operating input range
- Adjustable Frequency from 50kHz to 500kHz Operation
- Precision Reference Voltage (1.2 V)
- Programmable Soft−Start with Pre-biased Load Capability
- Programmable EN Off Delay Function
- Programmable Over-Load Protection with 0.2s blank timer and Hiccup
- Programmable Cycle-by-Cycle Current Limiting Protection
- Programmable Input Under-Voltage Lockout Protection with Latch
- Programmable Input Over-Voltage Protection with Latch
- Output Over-Voltage Protection
- Over-Temperature Protection
- QFN3x3-20 packages

2 Applications

- 48 V Non−Isolated DC−DC Converter
- Car applications
- Telecom Bus Converters
- General purpose
- USB Type-C Power Delivery
- Industrial DC-DC Motor Drivers

3 Description

LYF5805 is a high voltage PWM controller designed for high performance synchronous Buck DC/DC applications with input voltages up to 100V.

LYF5805 drives a pair of external NMOSFETs. The switching frequency is programmable from 50 kHz up to 500 kHz allowing the flexibility to tune for efficiency and size. The output voltage can be precisely regulated using the internally 1.2V reference voltage for low voltage applications.

Protection features include user programmable under voltage lockout, over voltage lockout and over current protection. The supply current drops below 10μA in shutdown mode. LYF5805 is a good choice for car infotainment application, telecom bus converter, etc.

4 Typical Application Schematic

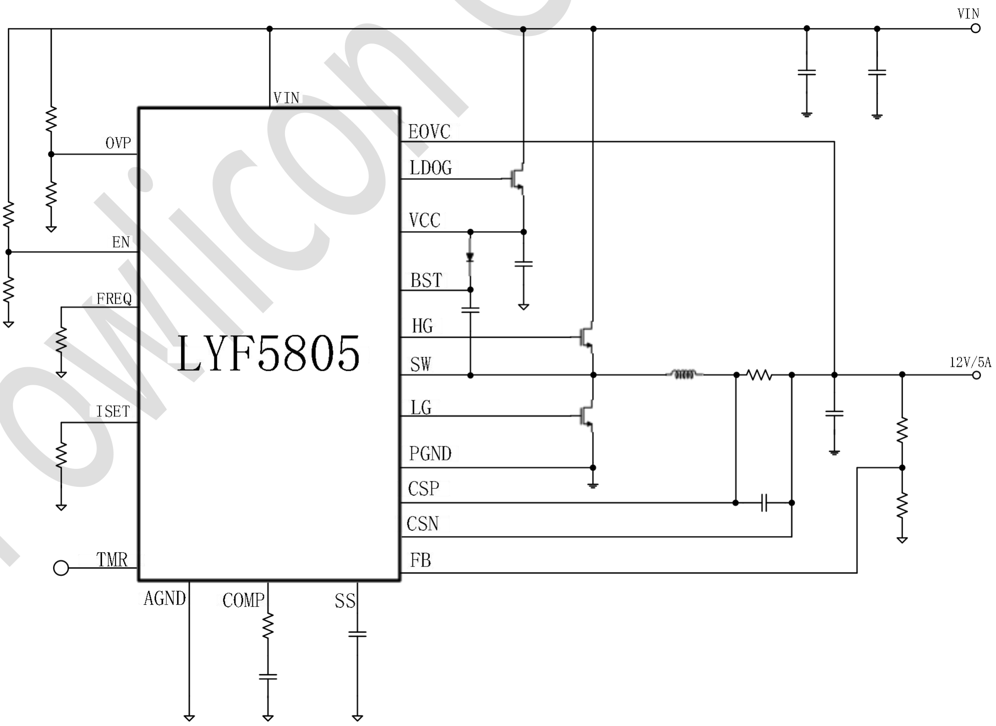


Fig. 1 Application Schematic

5 Pin Configuration and Functions

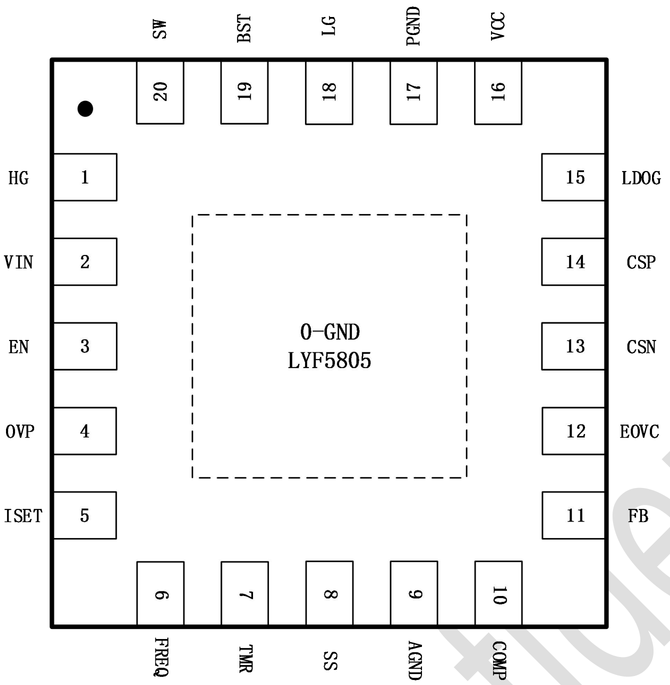


Fig. 2 QFN3x3-20 Package (Top View)

Pin		Description
Number	**Name**	
1	HG	Output driver for high side MOSFET.
2	VIN	Input voltage.
3	EN	Enable pin.
4	OVP	An external voltage divider is used to set the over voltage threshold levels.
5	ISET	Current limit set point. A resistor from this pin to GND will set the positive and negative current limit threshold.
6	FREQ	Connect this pin to GND by a resistor to set the switching frequency.
7	TMR	This pin provides user programmable shutdown delay time function. Connect to GND: No Delay Connect to VCC: 20s Floating: 10s
8	SS	This pin provides user programmable soft−start function. External capacitor connected from this pin to ground sets the startup time of the output voltage.
9	AGND	Signal ground for internal reference and control circuitry.
10	COMP	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
11	FB	Feedback Input. FB senses the output voltage. Connect FB with a resistor divider connected between the output and ground. FB is a sensitive node. Keep FB away from noisy signal, such as SW and BST pin.
12	EOVC	External Power Input to an Internal LDO linear regulator Connected to VCC. This LDO supplies VCC power from EOVC, bypassing the external LDOG LDO whenever EOVC is higher than 10V. Do not exceed 30V on this pin. Do not connect EOVC to a voltage greater than VIN. Connect to GND if not used.
13	CSN	Inductor current sense input 2.
14	CSP	Inductor current sense input 1.
15	LDOG	Drive Output for External Pass Device of the LDOG LDO Linear Regulator for VCC. Connect this pin to the gate of an external NMOS pass device.
16	VCC	This pin provides power for the internal blocks of the IC. A minimum of 4.7uFcapacitor must be connected from this pin to ground.
17	PGND	Power Ground. This pin serves as a separate ground for the MOSFET driver and should be connected to the system's power ground plane.
18	LG	Output driver for low side MOSFET.

19	BST	This pin powers the high side driver and must be connected to a voltage higher than input voltage. A minimum of 0.1uF, high frequency capacitor must be connected from this pin to switch node.
20	SW	Switch Node. This pin is connected to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is return path for the upper gate driver.

6 Device Marking Information

Order Information	Label Part NO.	Package	Package Qty	Top Marking
LYF5805	LYF5805IQF20A	QFN3x3-20	5000	5805 RAAYMD

LYF5805: Part Number
RAAYMD: RAA: LOT NO.; YMD: Package Date Code

7 Specifications

7.1 Absolute Maximum Ratings(Note1)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	-0.3	100	V
	V_{FB}, V_{OVP}, V_{UVLO} to GND	-0.3	6	
	V_{TOFF} to GND	-0.3	12	
	$V_{CSP,2}$ to GND	-0.3	65	
	V_{EN} to GND	-0.3	100	
	V_{EOVC} to GND	-0.3	30	
Output Voltages	V_{VCC} to GND	-0.3	20	V
	V_{FREQ}, V_{ISET}, V_{SS}, V_{COMP} to GND	-0.3	6	
	V_{LDRV} to GND	-0.3	20	
	V_{HDRV} to V_{SW}	-0.3	20	
	V_{BST} to V_{SW}	-0.3	20	
	V_{SW} to GND	-3	V_{IN}+ 0.3	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+150	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model		2	kV
	CDM Charger device model		500	V

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	12	100	V
	V_{FB}, V_{OVP}, V_{UVLO} to GND	-0.3	5	
	V_{TOFF} to GND	-0.3	10	
	$V_{CSP,2}$ to GND	-0.3	60	
	V_{EN} to GND	-0.3	100	
	V_{EOVC} to GND	-0.3	30	
Output Voltages	V_{VCC} to GND	-0.3	10	V
	V_{FREQ}, V_{ISET}, V_{SS}, V_{COMP} to GND	-0.3	5	
	V_{LDRV} to GND	-0.3	10	
	V_{HDRV} to V_{SW}	-0.3	10	
	V_{BST} to V_{SW}	-0.3	10	
	V_{SW} to GND	-3	V_{IN}+0.3	
Temperature	Operating junction temperature range, T_J	-40	+125	°C

7.4 Thermal Information(Note 4)

Symbol	Description	QFN3x3-20	Unit
θ_{JA}	Junction to ambient thermal resistance	44	°C/W
θ_{JC}	Junction to case thermal resistance	9	

Notes:

1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1” square of 1 oz copper

7.5 Electrical Characteristics(Typical at Vin = 48V, T_J=25°C, unless otherwise noted.)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VIN	Input Supply Operating Voltage Range		12		100	
VOUT	Regulated Output Voltage Set Point		1.2		60	
REFERENCE VOLTAGE						
I_Q	Statics Current	Open Loop, VFB = 1.25V, No Switching, VIN=48V , TJ=25℃		400		uA
$I_{SHUTDOWN}$	EN Shutdown Supply Current	Close Loop, VEN=0V, VIN=48V		20		
REFERENCE VOLTAGE						
V_{FB}	Feedback Voltage			1.2		V
	Accuracy		-1.5		+1.5	%
SUPPLY VOLTAGE (V_{CC})						
Vcc	V_{CC} Regulator Output	Supply by LDOG LDO	9	9.5	10	V
		Supply by EOVC LDO	9.5	10	10.5	V
UNDERVOLTAGE LOCKOUT						
V_{CC_UVLO}	V_{CC} Under Voltage Lockout Voltage(V_{CC} increasing)	-40°C≤ T_J≤ 125°C		8		V
V_{CC_UVLOH}	V_{CC} Under Voltage Hysteresis			670		mV
V_{BST_UVLO}	V_{BST} Under Voltage Lockout Voltage(V_{BST} increasing)	-40°C≤ T_J≤ 125°C		5.6		V
V_{BST_UVLOH}	V_{BST} Under Voltage Hysteresis			860		mV
V_{IN_UVLO}	VIN Under Voltage Lockout Voltage(V_{IN} increasing)			6.5		V
V_{IN_UVLOH}	VIN Under Voltage Hysteresis			650		mV
V_{EN_UVLO}	EN Under Voltage Lockout Voltage(V_{EN} increasing)			1.2		V
V_{EN_UVLOH}	EN Under Voltage Hysteresis			200		mV
OVER VOLTAGE LOCKOUT						
REF_{IN_OVP}	Reference of VIN Over Voltage Lockout Voltage(V_{IN} increasing)			1.2		V
HYS_{IN_OVP}	Reference Hysteresis of VIN Over Voltage Lockout Voltage			200		mV
CONTROL LOOP						
I(Source/ Sink)	Source/Sink Current			300		uA
gm	Trans-conductance			3		mS
SOFT−START						
I_{SS}	Soft−Start Current	SS = 0 V	15	20	25	uA
VSNS LIMIT						
V_{ISET}	ISET voltage	-40°C≤ T_J≤ 125°C		1.2		V
VLIMH	On Duty CSP-CSN Limit	R_{ISET} = 25k Ohm, VLIMH=1.2/R_{ISET}*25K/10		120		mV
VLIML	Off Duty CSP-CSN Limit	R_{ISET} = 25k Ohm, VLIML=1.2/R_{ISET}*20K/10		96		mV
$T_{OVERLOAD}$	Over Load Protection Blank Time			200		ms
Frequency						
F_{SW}	Switching Frequency	Fsw=Vout/(Rh*500p) or Fsw=1/(RL*50p)	50	200	500	kHz

TON_{MIN}	Minimum On Time		140	ns
$TOFF_{MIN}$	Minimum Off Time		400	ns
Toff Timer				
TOFF	Toff Time Delay	Toff = GND	0	s
		Toff = Float	10	s
		Toff = VCC	20	s
OUTPUT DRIVERS				
HG	Peak HG Source Current		1	A
	Peak HG Sink Current		2.2	A
LG	Peak LG Source Current		1.8	A
	Peak LG Sink Current		3.5	A
Tr(HG)	CLOAD = 1000pF		19	ns
Tf(HG)	CLOAD = 1000pF		13	ns
Tr(LG)	CLOAD = 1000pF		18	ns
Tf(LG)	CLOAD = 1000pF		12	ns
Tdelay1	Top Gate Off to Bottom Gate On Delay		70	ns
Tdelay2	Bottom Gate Off to Top Gate On Delay		70	ns

Note:
4) Guaranteed by design, not tested in production.

7.6 Typical Characteristics

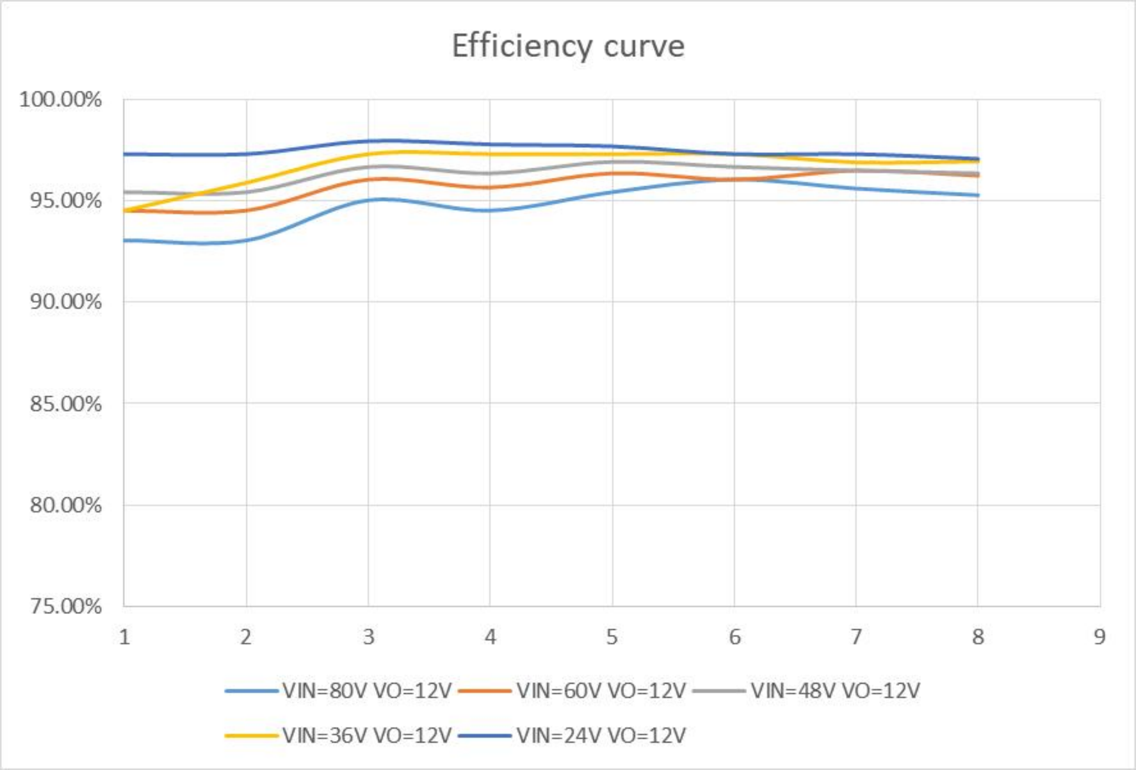
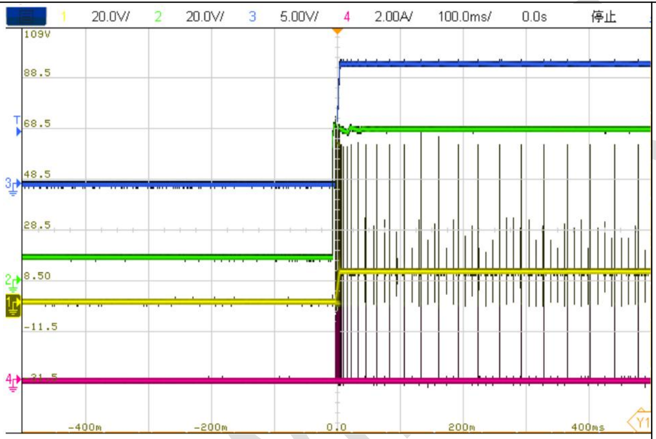


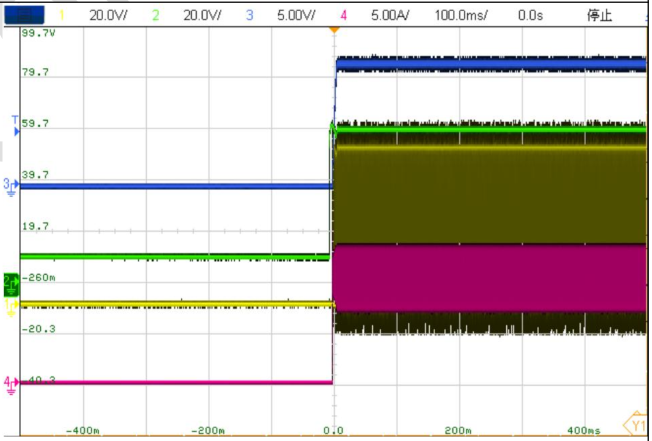
Fig. 3



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=60V Vout=12V

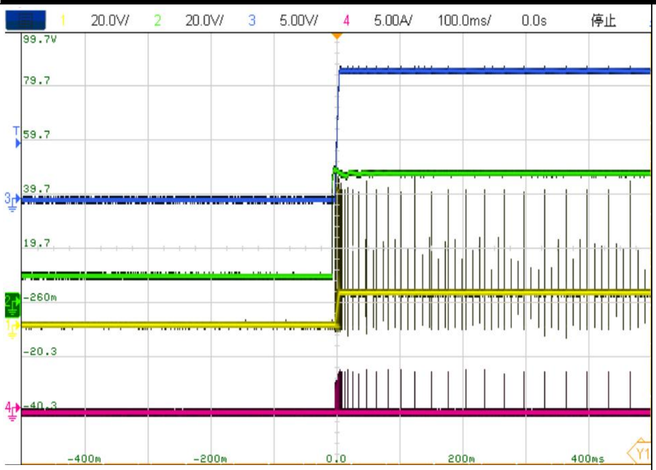
Fig. 4 Start up waveform through Vin, Iout =0A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=60V Vout=12V

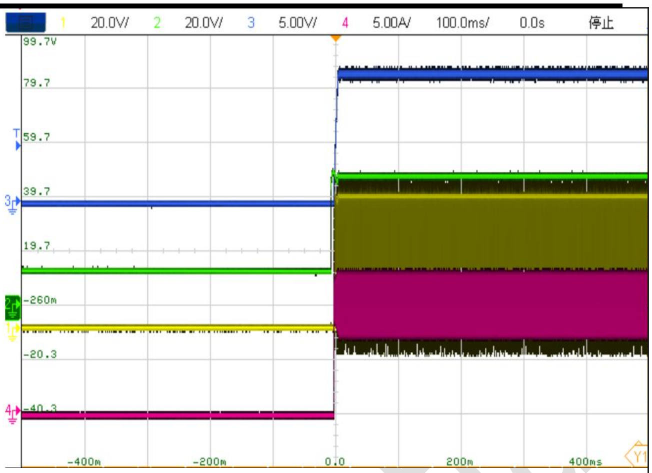
Fig. 5 Start up waveform through Vin, Iout =10A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=48V Vout=12V

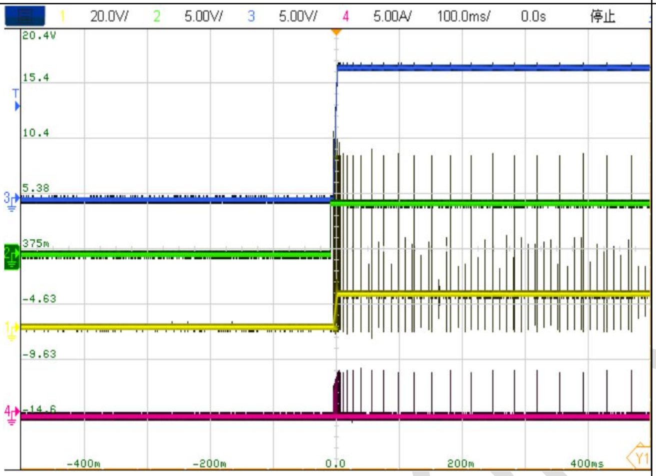
Fig. 6 Start up waveform through Vin, Iout =0A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=48V Vout=12V

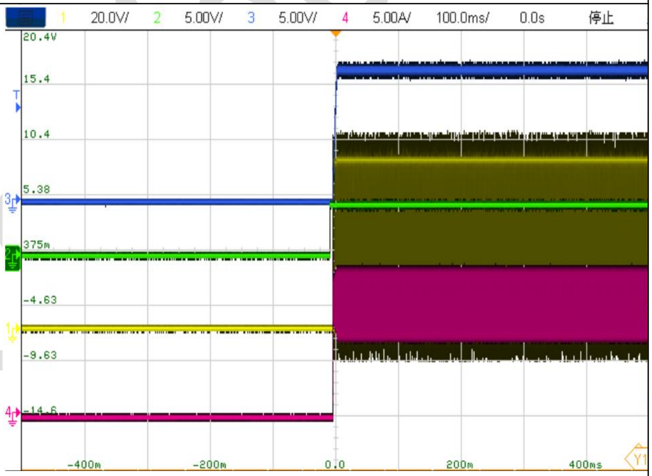
Fig. 7 Start up waveform through Vin, Iout =10A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=60V Vout=12V

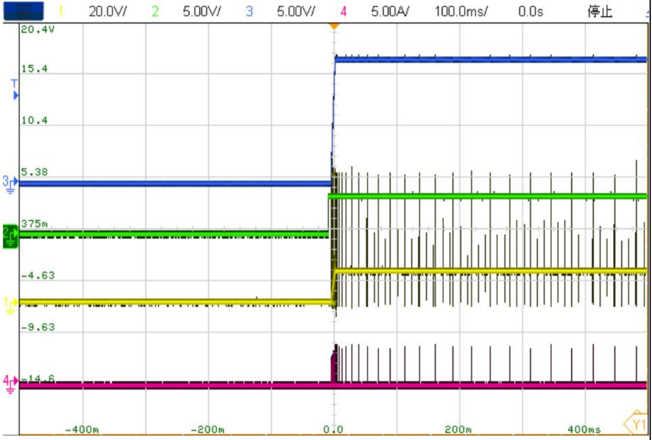
Fig. 8 Start up waveform through EN, Iout =0A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=60V Vout=12V

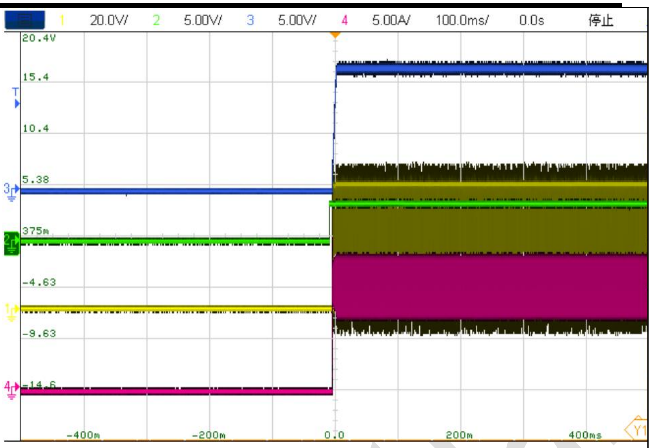
Fig. 9 Start up waveform through EN, Iout =10A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=48V Vout=12V

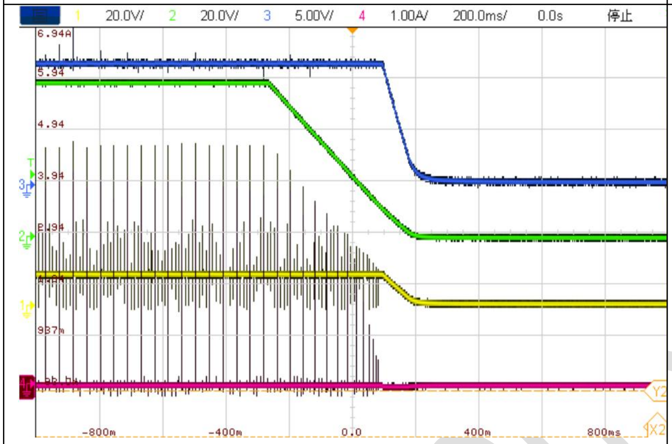
Fig. 10 Start up waveform through EN, Iout =0A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=48V Vout=12V

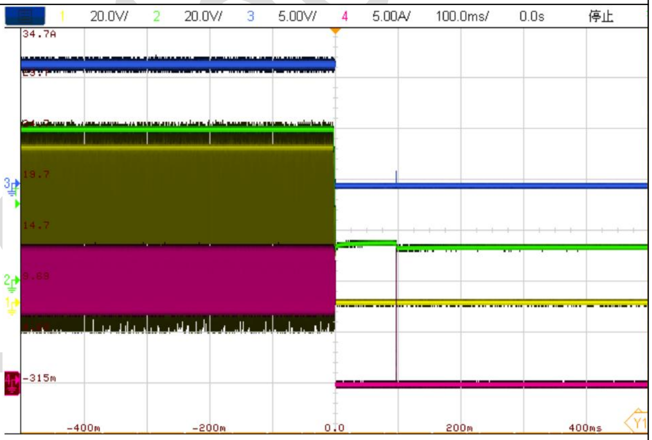
Fig. 11 Start up waveform through EN, Iout =10A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=60V Vout=12V

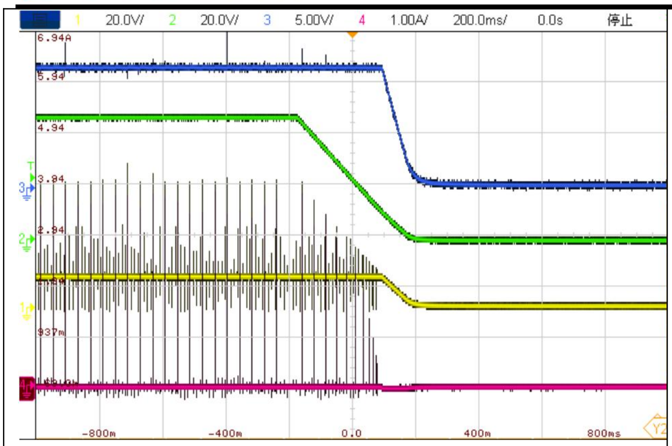
Fig. 12 Shut Down waveform through VIN, Iout =0A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=60V Vout=12V

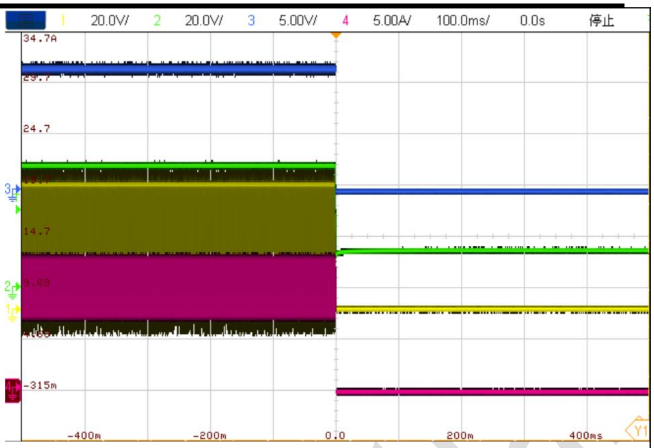
Fig. 13 Shut Down waveform through VIN, Iout =10A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=48V Vout=12V

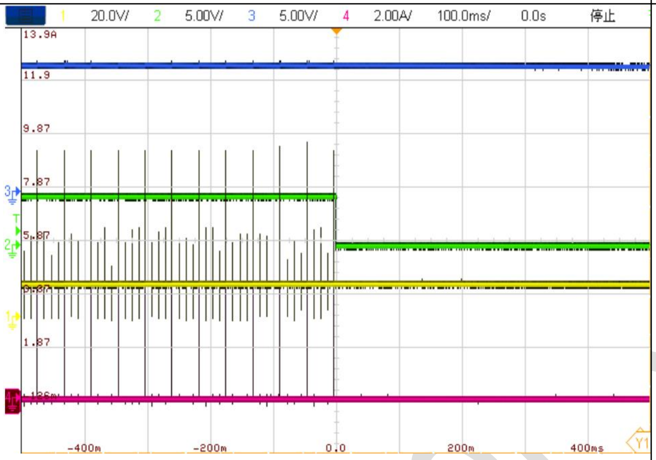
Fig. 14 Shut Down waveform through VIN, Iout =0A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=48V Vout=12V

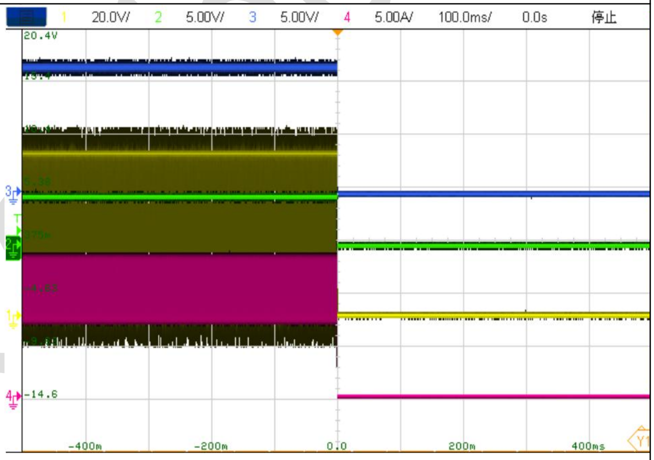
Fig. 15 Shut Down waveform through VIN, Iout =10A



CH1: SW CH2:EN CH3:VOUT CH4:IL

Vin=60V Vout=12V

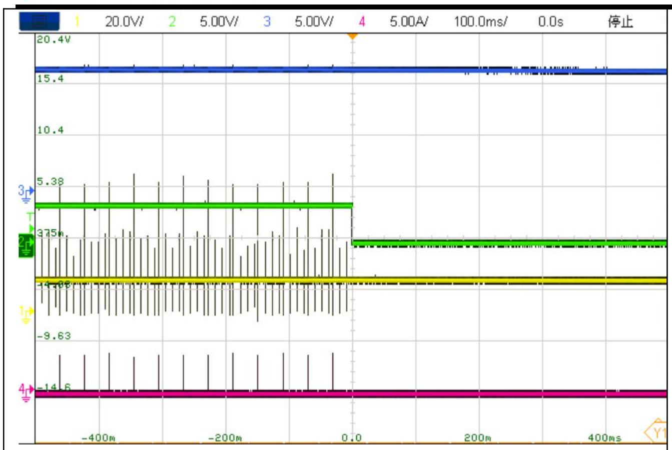
Fig. 16 Shut Down waveform through EN, Iout =0A



CH1: SW CH2:EN CH3:VOUT CH4:IL

Vin=60V Vout=12V

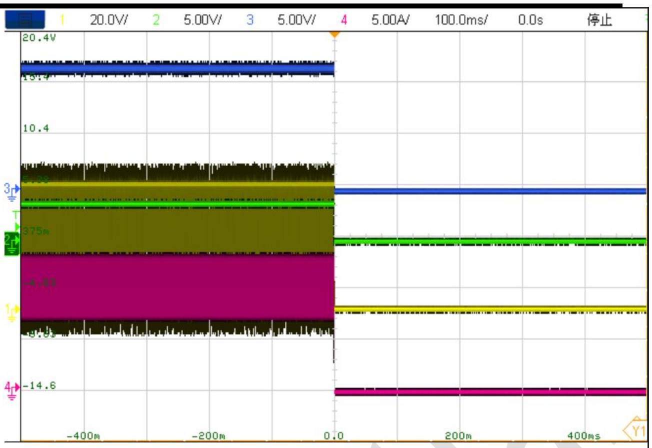
Fig. 17 Shut Down waveform through EN, Iout =10A



CH1: SW CH2:EN CH3:VOUT CH4:IL

Vin=48V Vout=12V

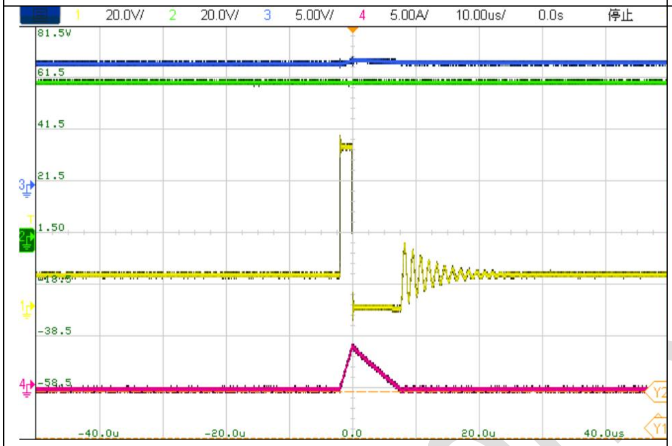
Fig. 18 Shut Down waveform through EN, Iout =0A



CH1: SW CH2:EN CH3:VOUT CH4:IL

Vin=48V Vout=12V

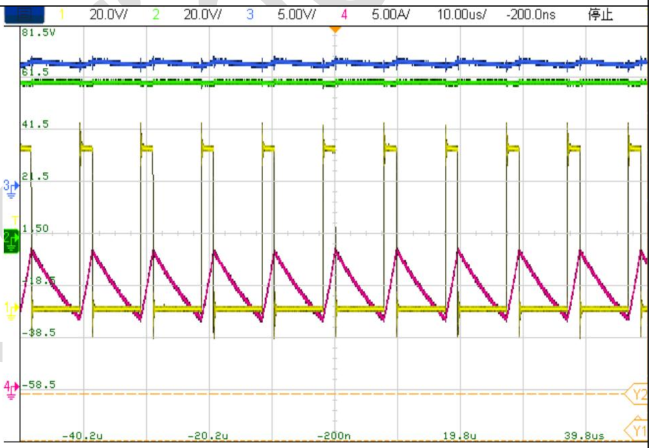
Fig. 19 Shut Down waveform through EN, Iout =10A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=60V Vout=12V

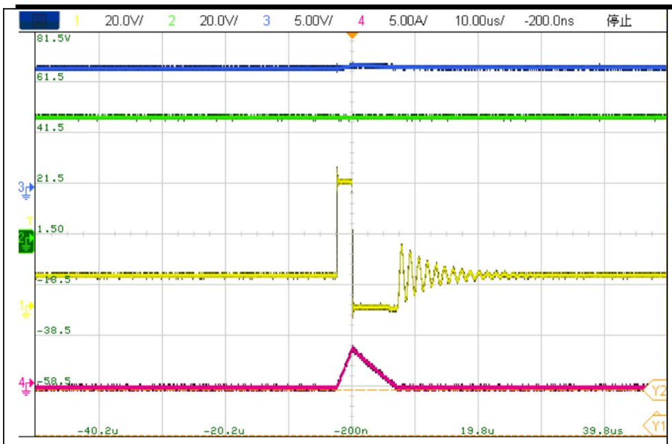
Fig. 20 Steady State waveform Iout =0A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=60V Vout=12V

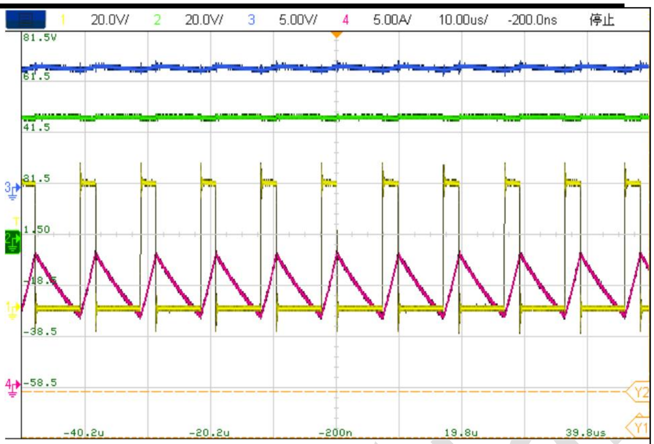
Fig. 21 Steady State waveform Iout =10A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=48V Vout=12V

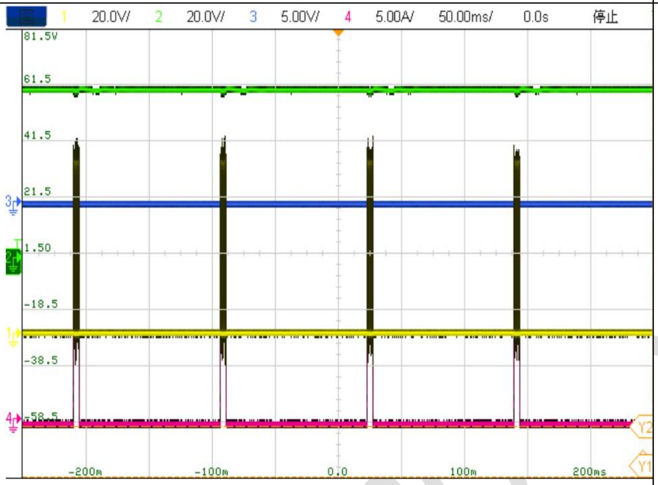
Fig. 22 Steady State waveform Iout =0A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=48V Vout=12V

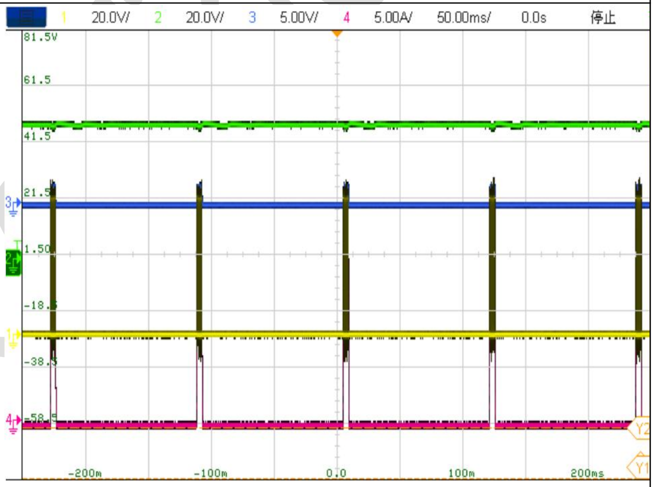
Fig. 23 Steady State waveform Iout =3A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=60V Vout=12V

Fig. 24 Short Circuit waveform Iout =10A



CH1: SW CH2:VIN CH3:VOUT CH4:IL

Vin=48V Vout=12V

Fig. 25 Short Circuit waveform Iout =10A

8 Detailed Description

8.1 Overview

The LYF5805 is a high voltage PWM controller designed for high performance synchronous Buck DC/DC applications with input voltages up to 100V. The LYF5805 adopts adaptive constant on time peak current mode control at the moderate to heavy load currents and operates in the PFM mode at the light load current. With this control scheme, the LYF5805 provides the excellent line and load transient response with the minimal output capacitor. The external loop compensation brings the flexibility to use a wider range of the inductor and output capacitor combinations.

The LYF5805 supports the adjustable switching frequency up to 500kHz. This device implements user programmable cycle-by-cycle current limit with 200ms over load timer to protect the device from thermal run away. If the overload condition is triggered, this part will stop switching until EN is toggled. This device also implements user programmable over voltage lockout protection and over temperature protection to ensure reliably operation.

8.2 Functional Block Diagram

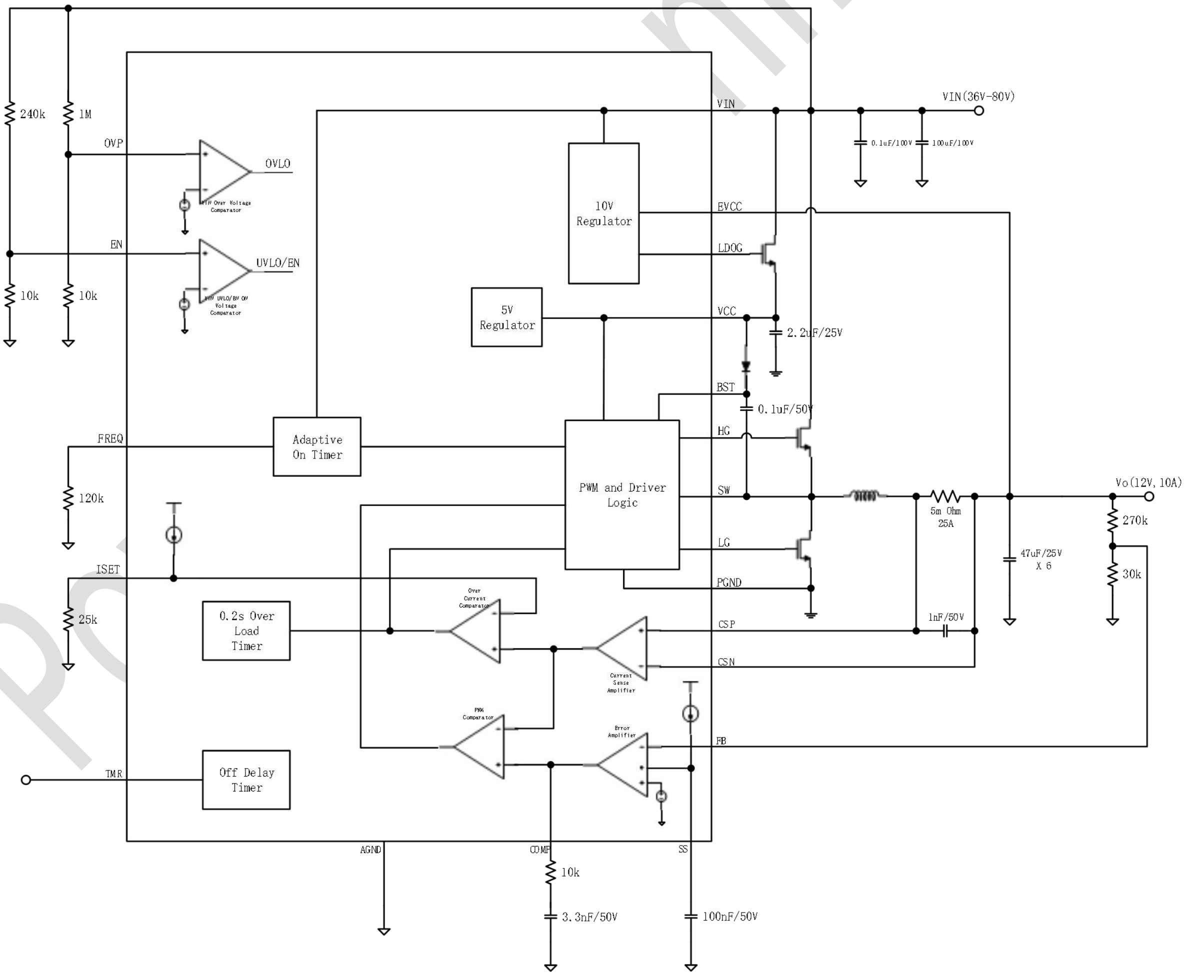


Fig. 26 Functional Block Diagram

8.3 Feature Description

8.3.1 Enable and OVP

When the EN pin is pulled high above 1.2V, this part is enabled. When the EN pin is pulled below 1.0V, this part goes into the shutdown mode and stops operation.

When the OVP pin is pulled high above 1.2V, the LYF5805 is disabled and it will not resume switching even if OVP falls below 1.0V unless EN is toggled.

8.3.2 Under-voltage Lockout

This controller stops switching when the input voltage drops below 5.85V or VCC is below 7.33V. It resumes operation when input voltage is larger than 6.5V and VCC is larger than 8V.

8.3.3 Cycle-by-Cycle Current Limit and Over Load Protection

The LYF5805 provides cycle-by-cycle current limit to protect power MOSFET during on duty and also off duty. It will immediately turn off high side MOSFET once on duty current limit is triggered or prolongs the off duty until the inductor current is lower than off duty current limit. Hiccup protection will be triggered if the over current condition endures more than 200ms. And the switching will be resumed after 16 soft start procedures.

8.3.4 Programmable Switching Frequency

This controller features a programmable switching frequency ranging from 50kHz to 500kHz.

The frequency setting by FREQ is calculated as below:

$$F_{SW} = \frac{V_{OUT}}{R_{FREQ}(k\Omega) \times 0.5}(\mathrm{MHz}) \qquad (1)$$

8.3.5 Error Amplifier

The LYF5805 has a trans-conductance amplifier and compares the feedback voltage with the internal voltage reference (or the internal soft start voltage during startup phase). The trans-conductance of the error amplifier is 3 mA / V typically. The loop compensation components are required to be placed between the COMP terminal and ground to balance the loop stability and the transient response time.

8.3.6 VCC Regulators

The LYF5805 contains two VCC regulators that provide power supply for low side gate driver and boot-strap high side gate drive. One is the LDOG regulator which regulates VCC to 9.5V. The other one is the 10V low dropout LDO powered by EOVC which is current limited to 60mA. The VCC load current should be evaluated if LDOG regulator is not used.

8.3.7 Bootstrap Voltage (BST)

The LYF5805 has an integrated bootstrap regulator, and requires a small ceramic capacitor between the BST pin and SW pin to provide the gate drive voltage for the high-side FET. The bootstrap capacitor is charged when the BST-SW voltage is below regulation. The value of this ceramic capacitor should be above 100 nF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 25 V or higher is recommended because of the stable characteristics over temperature and DC biased voltage.

8.3.8 Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 150°C. When the thermal shutdown is triggered, the device stops switching and recover when the junction temperature falls below 130°C.

9 Application and Implementation

9.1 Setting the switching Frequency

The switching frequency of the LYF5805 can be programmed as equation 1. For a target switching frequency of 200 kHz, The calculated value is 120 kΩ.

9.2 Setting the Output Current Limit

The cycle-by-cycle current limit of the LYF5805 is configured by combination of RISET between ISET and AGND and sense resistor Rsns in serial with inductor. The cycle-by-cycle current limit is determined as follows:

$$I_{LIML} = \frac{2.4}{R_{ISET}(k\Omega) \times R_{SNS}(\Omega)}(A) \tag{2}$$

9.3 Setting the Output Voltage

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R1 and R2. A value between 10k and 1M is recommended for both resistors. If R1=200k is chosen, then R2 can be calculated to be:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \tag{3}$$

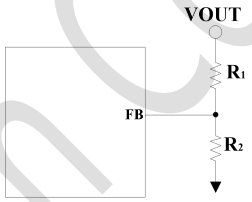


Fig. 27

9.4 Selecting the Inductor

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN} - V_{OUT}}{0.4 \times F_{SW} \times I_{OUT\_MAX}} \tag{4}$$

where F_{SW} is the switching frequency and $I_{OUT_MAX}$is the maximum load current.

LYF5805 is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve a good over -all efficiency.

9.5 Selecting the Output Capacitors

The Output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken in to account when selecting these capacitors. For the best performance, it is recommended to use X5R or better grade ceramic capacitor.

9.6 Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-down converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 10-μF input capacitor is sufficient for the most applications, larger values may be used to reduce input current ripple.。

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, should be placed between CIN and the power source lead to reduce ringing that can occur between the inductance of the power source leads and CIN.

9.7 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during each cycle’s turn-on and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1μF to 1μF. CBST should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1μF was selected for this design example.

9.8 Selecting the VCC Capacitors

The primary purpose of the VCC capacitor is to supply the peak transient currents of the driver and bootstrap capacitor as well as provide stability for the VCC regulator. The value of CVCC should be at least 10 times greater than the value of CBST, and should be a good quality, low ESR, ceramic capacitor. CVCC should be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 4.7μF was selected for this design example.

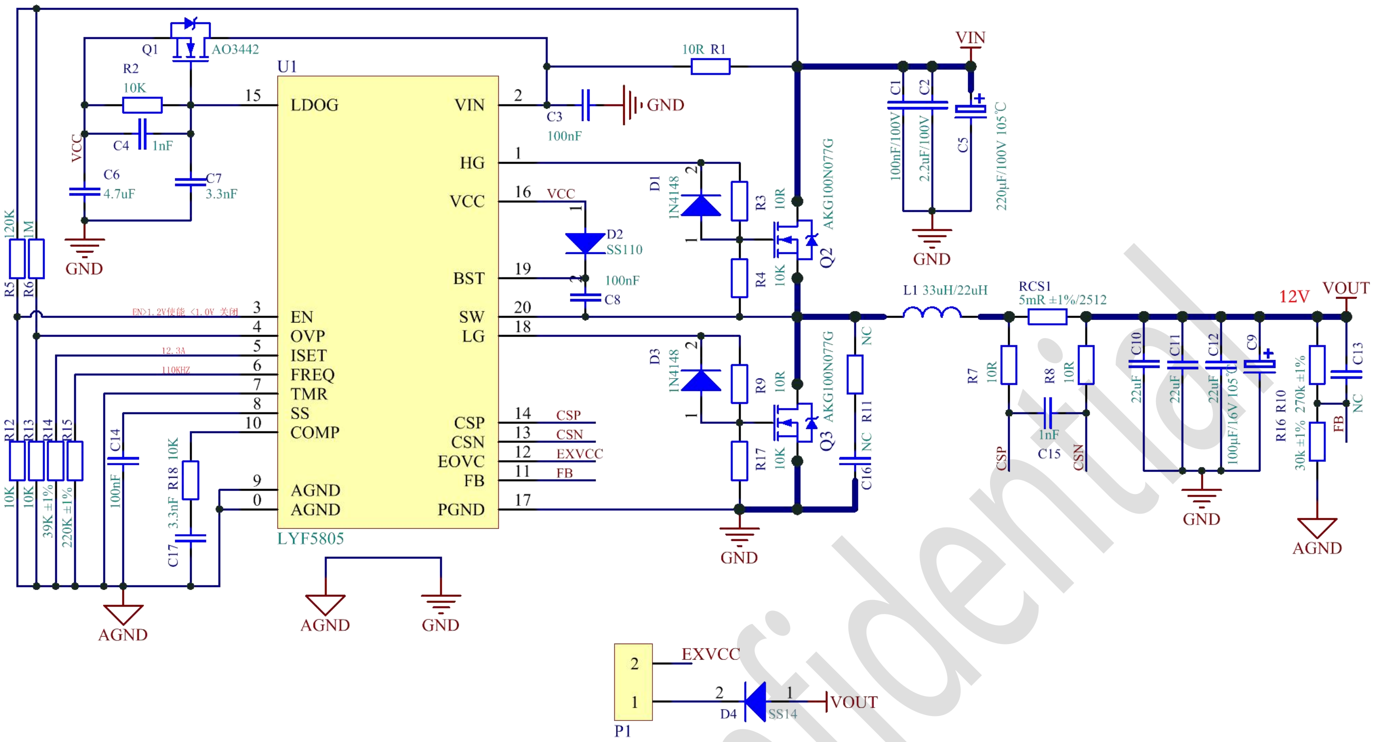
9.9 Selecting the MOSFET

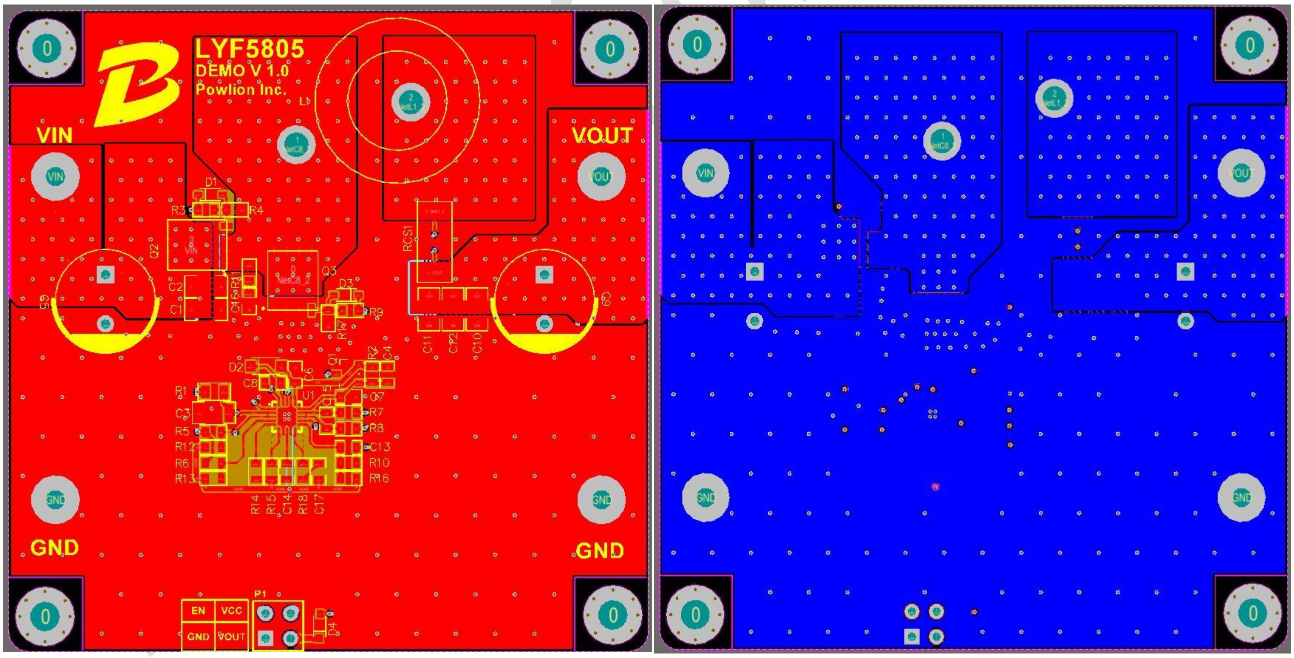
Important parameters for MOSFET selection are:

- Voltage rating
- On-resistance
- Total gate charge

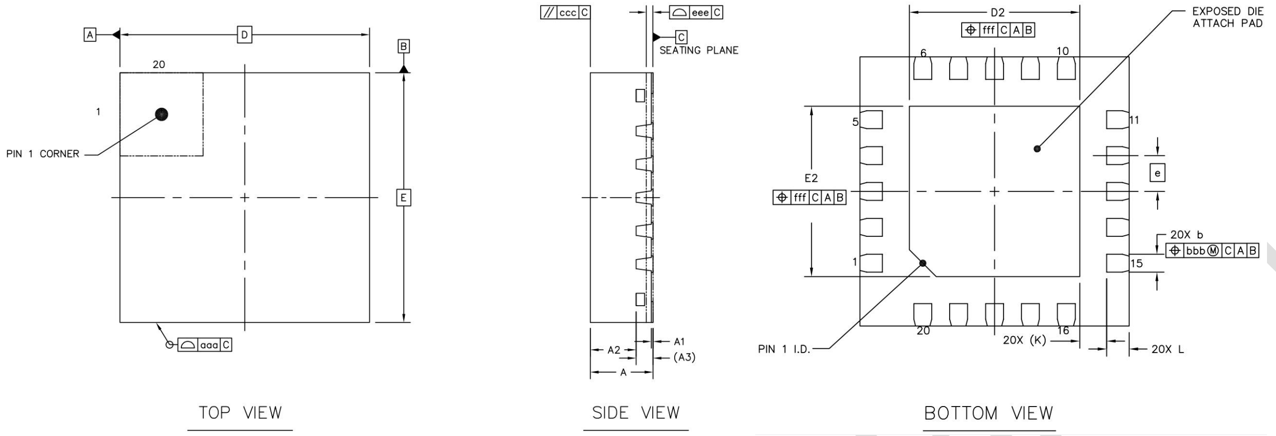
The voltage rating for the high-side and low-side MOSFETs are essentially equal to the power stage input voltage VIN. A safety factor of 30% should be added to the VIN(MAX).

9.10 Application Examples





10 Packaging Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	3 BSC		
	Y	E	3 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	D2	1.8	1.9	2
	Y	E2	1.8	1.9	2
LEAD LENGTH		L	0.15	0.25	0.35
LEAD TIP TO EXPOSED PAD EDGE		K	0.3 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.07		
EXPOSED PAD OFFSET		fff	0.1		

IMPORTANT NOTICE