PL3900 100V Multi-Phase Synchronous Buck/Boost Controller

1 Features

- 2-Phase Operation Reduces Required Input and Output Capacitance and Power Supply Induced Noise
- Synchronous Operation for Highest Efficiency and Reduced Heat Dissipation
- Wide VIN Range:4.5V to 56V (Sense Pin 60V Abs Max) in Boost mode and Operates Down to 2.5V After Start-Up ， 4.5V to 96V (Vbias Pin 100V Abs Max) in Buck mode
- Output Voltage Up to 96V(Boost mode) and 56V(Buck mode)
- ±1% 1.2V Reference Voltage
- RSENSE or Inductor DCR Current Sensing
- CV/CC Mode control (Constant voltage and constant current)
- Phase-Lockable Frequency (75kHz to 850kHz).
- Programmable Fixed Frequency (50kHz to 900kHz)
- Power Good Output Voltage Monitor
- Internal LDO Powers Gate Drive from VBIAS or EXTVCC
- Thermally Enhanced Low Profile 28-Pin 4mm × 5mm QFN Package

2 Applications

- consumer
- Industrial
- Automotive
- Medical

3 Description

The PL3900 is a high performance Multi-Phase single output synchronous buck/boost converter controller that drives two N-channel power MOSFET stages out-of-phase. Multiphase operation reduces input and output capacitor requirements and allows the use of smaller inductors than the single-phase equivalent. Synchronous rectification increases efficiency, reduces power losses and eases thermal requirements, enabling high power boost applications.

A 4.5V to 56V (boost mode) and 4.5V to 96V (buck mode) input supply range encompasses a wide range of system architectures and battery chemistries. When biased from the output of the converter or another auxiliary supply, the PL3900 can operate from an input supply as low as 2.5V after start-up. The operating frequency can be set for a 50kHz to 900kHz range or synchronized to an external clock using the internal PLL. Multi-Phase operation allows the PL3900 to be configured for 2-, 3-, 4-, 6- and 12-phase operation.

The SS pin ramps the output voltage during start-up. The PLLIN/MODE pin selects Burst Mode operation, pulse-skipping mode or forced continuous mode at light loads.

4 Typical Application Schematic

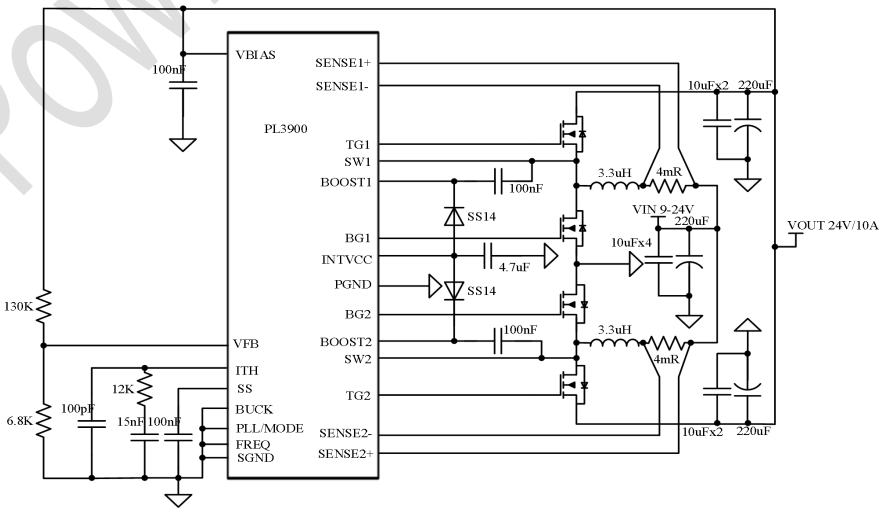


Fig4 Typical Application Schematic

5 Pin Configuration and Functions

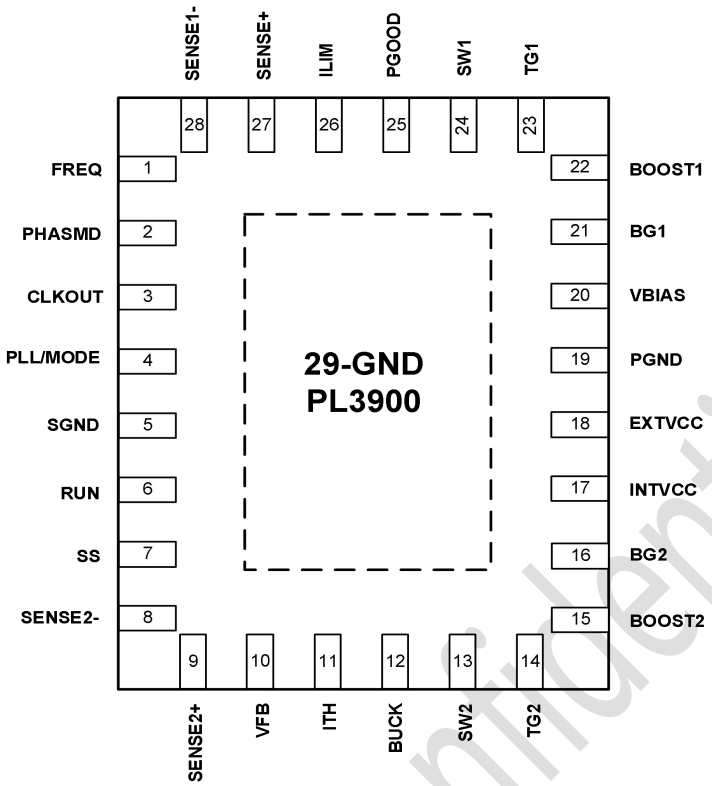


Fig5 Pin-Function

Pin		Description
Number	Name	
1	FREQ	Frequency Control Pin for the Internal VCO. Connecting the pin to SGND forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to INTVCC forces the VCO to a fixed high frequency of 535kHz. The frequency can be programmed from 50kHz to 900kHz by connecting a resistor from the FREQ pin to SGND.
2	PHASMD	This pin can be floated, tied to SGND, or tied to INTVCC to program the phase relationship between the rising edges of BG1 and BG2, as well as the phase relationship between BG1 and CLKOUT.
3	CLKOUT	A Digital Output Used for Daisy-chaining Multiple PL3900 ICs in Multiphase Systems. The PHASMD pin voltage controls the relationship between BG1 and CLKOUT. This pin swings between SGND and INTVCC.
4	PLLIN/MODE	External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, it will force the controller into forced continuous mode of operation and the phase-locked loop will force the rising BG1 signal to be synchronized with the rising edge of the external clock. When not synchronizing to an external clock, this input determines how the PL3900 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to INTVCC forces continuous inductor current operation. Tying this pin to a voltage greater than 1.2V and less than INTVCC-1.3V selects pulse-skipping operation. This can be done by adding a 100k resistor between the PLLIN/ MODE pin and INTVCC.
5	SGND	Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at a single point.
6	RUN	Run Control Input. Forcing this pin below 1V shuts down the entire PL3900, An external resistor divider connected to VIN can set the threshold for converter operation.
7	SS	Output Soft-Start Input. A capacitor to ground at this pin sets the ramp rate of the output voltage during start-up.
8	SENSE2–	Negative Current Sense Comparator Input.

9	SENSE2+	Positive Current Sense Comparator Input. This pin also supplies power to the current comparator. The common mode voltage range on SENSE+ and SENSE–pins is 2.5V to 56V (60V abs max).
10	VFB	Error Amplifier Feedback Input. This pin receives the remotely sensed feedback voltage from an external resistive divider connected across the output.
11	ITH	Current Control Threshold and Error Amplifier Compensation Point. The voltage on this pin sets the current trip threshold.
12	BUCK	This pin connect to Ground or Float to set PL3900 in Boost mode. This pin connect INTVCC pin to set PL3900 in buck mode.
13	SW2	Switch Node. Connect to the source of the synchronous N-channel MOSFET, the drain of the main N-channel MOSFET and the inductor.
14	TG2	Top Gate. Connect to the gate of the synchronous N-channel MOSFET.
15	BOOST2	Floating power supply for the synchronous N-channel MOSFET, Bypass to SW with a capacitor and supply with a Schottky diode connected to INTVCC.
16	BG2	Bottom Gate. Connect to the gate of the main N-channel MOSFET.
17	INTVCC	Output of Internal 5.4V LDO. Power supply for control circuits and gate drivers. De-couple this pin to GND with a minimum 4.7μF low ESR ceramic capacitor.
18	EXTVCC	External Power Input. When this pin is between 4.8V and 30V, an internal switch bypasses the internal regulator and supply power to INTVCC directly from EXTVCC. Do not float this pin. It can be connected to ground when not used.
19	PGND	Driver Power Ground. Connects to the sources of bottom (main) N-channel MOSFETs and the (–) terminal(s) of CIN and COUT.
20	VBIAS	Main Supply Pin. It is normally tied to the input supply VIN or to the output of the boost converter. A bypass capacitor should be tied between this pin and the signal ground pin. The operating voltage range on this pin is 4.5V to 96V (100V abs max).
21	BG1	Bottom Gate. Connect to the gate of the main N-channel MOSFET.
22	BOOST1	Floating power supply for the synchronous N-channel MOSFET, Bypass to SW with a capacitor and supply with a Schottky diode connected to INTVCC.
23	TG1	Top Gate. Connect to the gate of the synchronous N-channel MOSFET.
24	SW1	Switch Node. Connect to the source of the synchronous N-channel MOSFET, the drain of the main N-channel MOSFET and the inductor.
25	PGOOD	Power Good Indicator. Open drain logic output that is pulled to ground when the output voltage is more than ±10 % away from the regulated output voltage. To avoid false trips the output voltage must be outside the range for 25μs before this output is activated.
26	ILIM	Current Comparator Sense Voltage Range setting. This pin is used to set the peak current sense voltage in the current comparator. Connect this pin to INTVCC to set the peak current sense voltage to 60mV and the controller operates in constant voltage mode, Short circuit protection for hiccups can be achieved in buck mode. Connect this pin to SGND by a resistor to set the current sense voltage range and the controller operates in constant voltage and constant current mode.
27	SENSE1+	Positive Current Sense Comparator Input. This pin also supplies power to the current comparator. The common mode voltage range on SENSE+ and SENSE–pins is 2.5V to 56V (60V abs max).
28	SENSE1–	Negative Current Sense Comparator Input.
29	GND	Exposed pad of the package. Soldered to the Ground and connect to a large copper plane to reduce thermal resistance.

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL3900	PL3900IQN28A	QFN4X5-28L	5000	3900 RAAYMD

3900: Part Number
RAAYMD : RAA: LOT NO.; YMD: Package Date Code

7 Specifications

7.1 Absolute Maximum Ratings(Note1)

PARAMETER	MIN	MAX	Unit
VBIAS to GND	-0.3	100	V
BOOST1 and BOOST2 to GND	-0.3	100	
SW1 and SW2 to GND	-0.3	100	
RUN to GND	-0.3	6	
PGOOD, PLLIN/MODE to GND	-0.3	6	
INTVCC to GND, (BOOST1 - SW1), (BOOST2 - SW2	-0.3	6	
EXTVCC to GND	-0.3	30	
SENSE1+, SENSE1－, SENSE2+, SENSE2－ to GND	-0.3	60	
(SENSE1+ - SENSE1－), (SENSE2+ - SENSE2－)	-0.3	0.3	
ILIM, SS, ITH, FREQ, PHASMD, VFB to GND	-0.3	6	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
TST	Storage Temperature Range	-65	+150	°C
TJ	Junction Temperature	-40	+150	°C
VESD	HBM Human body model	2		kV

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
VBIAS Voltages	VBIAS	5.0	100	V
Temperature	Operating junction temperature range, TJ	-40	+150	°C

7.4 Thermal Information(Note 3)

Symbol	Description	QFN4X5-28L	Unit
θJA	Junction to ambient thermal resistance	43	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

7.5 Electrical Characteristics

The I denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at TA = 25°C, VBIAS = 12V, unless otherwise noted (Note 2).

Supply voltages	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VBIAS	Chip Bias Voltage Operating Range		4.5		100	V
VFB	Regulated Feedback Voltage	ITH = 1.2V		1.200		V
IQ	Input DC Supply Current Pulse-Skipping or Forced Continuous Mode	RUN = 5V; VFB = 1.25V (No Load)		1.2		mA
	Sleep Mode	RUN = 5V; VFB = 1.25V (No Load)		340		μA
	Shutdown	RUN = 0V		8		μA
UVLO	INTVCC Under voltage Lockout Thresholds	VINTVCC Ramping Up VINTVCC Ramping Down		4.1 3.8		V V
VRUN	RUN Pin ON Threshold	VRUN Rising	1	1.2		V
VRUNHYS	RUN Pin Hysteresis		200			mV
ISS	Soft-Start Charge Current	VSS = GND		10		μA
VSENSE1,2(MAX)	Maximum Current Sense Threshold	VFB = 1.1V, ILIM = INTVCC		60		mV
VSENSE(CM)	SENSE Pins Common Mode Range	Boost mode Buck mode	2.5 0		60 60	V V
ISENSE1,2+	SENSE+ Pin Current	VFB = 1.1V, ILIM = GND		200		μA
ISENSE1,2–	SENSE– Pin Current	VFB = 1.1V, ILIM = GND			±1	μA
tr(TG1,2)	Top Gate Rise Time	CLOAD = 3300pF		20		ns
tf(TG1,2)	Top Gate Fall Time	CLOAD = 3300pF		20		ns
tr(BG1,2)	Bottom Gate Rise Time	CLOAD = 3300pF		20		ns
tr(BG1,2)	Bottom Gate Fall Time	CLOAD = 3300pF		20		ns
RUP(TG1,2)	Top Gate Pull-Up Resistance			1.2		Ω
RDN(TG1,2)	Top Gate Pull-Down Resistance			1.2		Ω
RUP(TG1,2)	Bottom Gate Pull-Up Resistance			1.2		Ω
RDN(TG1,2)	Bottom Gate Pull-Down Resistance			1.2		Ω
tD(TG/BG)	Top Gate Off to Bottom Gate On Switch-On Delay Time	CLOAD = 3300pF (Each Driver)		70		ns
tD(BG/TG)	Bottom Gate Off to Top Gate On Switch-On Delay Time	CLOAD = 3300pF (Each Driver)		70		ns
DMAX	Maximum Duty Cycle			96		%
tON(MIN)	Minimum On-Time			110		ns
INTVCC Linear Regulator						
VINTVCC(VIN)	Internal VCC Voltage	6V < VBIAS < 56V, VEXTVCC = 0		5.4		V
VINTVCC(EXT)	Internal VCC Voltage	VEXTVCC = 6V		5.4		V
VEXTVCC	EXTVCC Switchover Voltage	EXTVCC Ramping Positive		4.8		V
VLDOHYS	EXTVCC Hysteresis		250			mV

Oscillator and Phase-Locked Loop						
fPROG	Programmable Frequency	RFREQ = 25k RFREQ = 60k RFREQ = 100k		105 400 760		kHz kHz kHz
fLOW	Lowest Fixed Frequency	VFREQ = 0V		350		kHz
fHIGH	Highest Fixed Frequency	VFREQ = INTVCC		535		kHz
fSYNC	Synchronizable Frequency	PLLIN/MODE = External Clock	75		850	kHz
tPGOOD(DELAY)	PGOOD Delay	PGOOD Going High to Low	25			μs
THERMAL SHUTDOWN						
TSD	Thermal shutdown threshold	TJ rising		150		°C
TSD-HYS	Thermal shutdown hysteresis		15			°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The PL3900 is tested under pulsed load conditions such that TJ ≈ TA. the PL3900 is guaranteed over the –40°C to 150°C operating temperature range . High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 150°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (TJ, in °C) is calculated from the ambient temperature (TA, in °C) and power dissipation (PD, in Watts) according to the formula: TJ = TA + (PD • JA), where JA = 43°C/W for the QFN package.

Note 3: This IC includes over temperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

8 Typical Characteristics

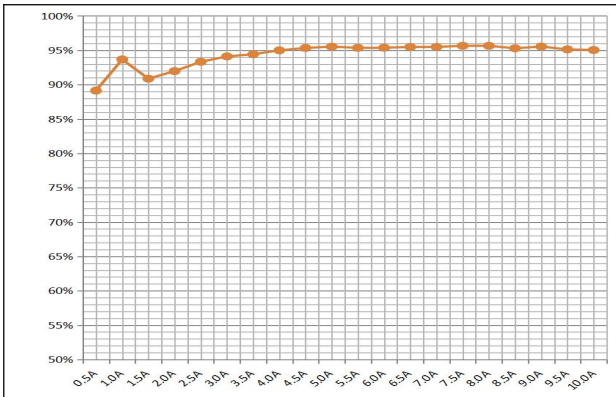


Fig8-1 Efficiency-Vin12V/Vout:24V

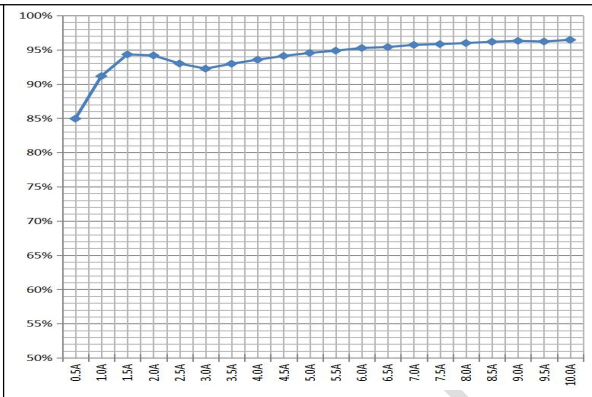
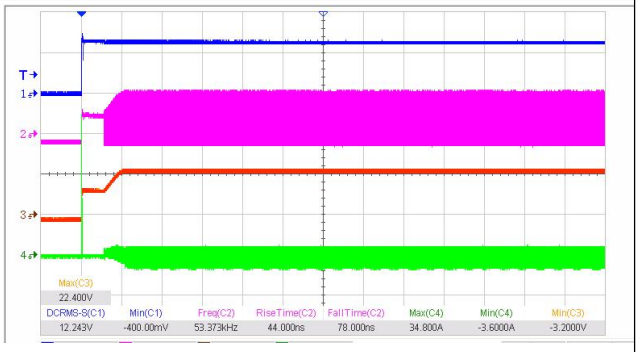
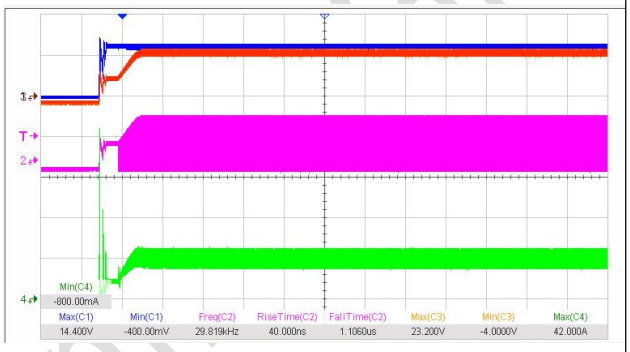


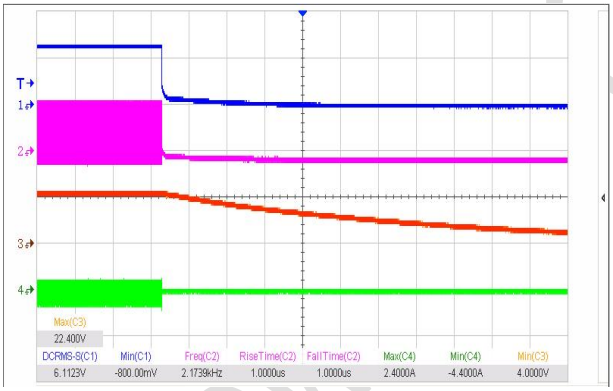
Fig8-2 Efficiency-Vin24V/Vout:36V



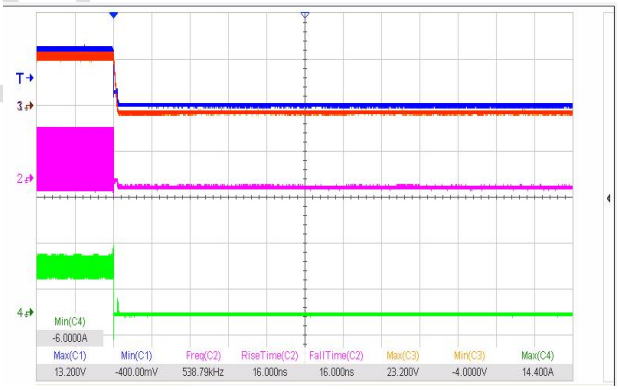
1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=12V Vout=24V
Fig8-3 Vin Start up waveform, Iout =0A



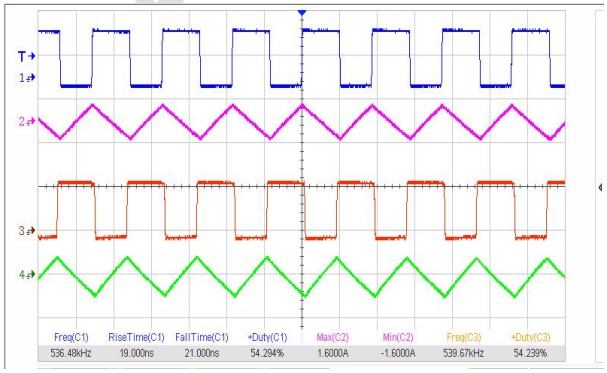
1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=12V Vout=24V
Fig8-4 Vin Start up waveform, Iout =10A



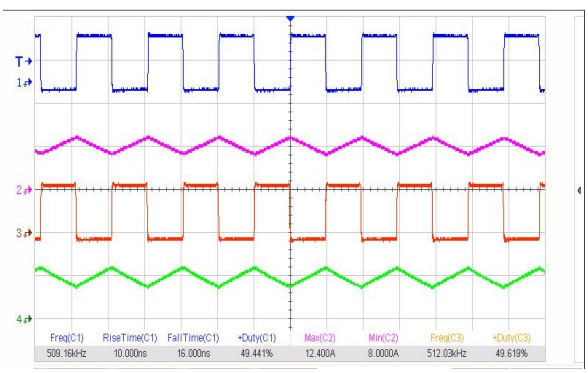
1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=12V Vout=24V
Fig8-5 Vin Shut down waveform, Iout =0A



1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=12V Vout=24V
Fig8-6 Vin Shut down waveform, Iout =10A



1#:SW1 2#:IL1 3#:SW2 4#:IL2
Vin=12V Vout=24V
Fig8-7 Steady State waveform, Iout =0A



1#:SW1 2#:IL1 3#:SW2 4#:IL2
Vin=12V Vout=24V
Fig8-8 Steady State waveform, Iout =10A

9 Detailed Descriptions

9.1Main Control Loop

The PL3900 uses a constant-frequency, current mode step-up and step-down architecture with two controller channels operating out of phase. During normal operation, each external bottom MOSFET is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier EA. The error amplifier compares the output voltage feedback signal at the VFB pin (which is generated with an external resistor divider connected across the output voltage, VOUT, to ground), to the internal 1.200V reference voltage. In a boost converter, the required inductor current is determined by the load current, VIN and VOUT.

9.2 Shutdown and Start-Up (RUN and SS Pins)

The two internal controllers of the PL3900 can be shut down using the RUN pin. Pulling this pin below 1V disables both controllers and most internal circuits, including the INTVCC LDOs. In this state, the PL3900 draws only 8μA of quiescent current.

The RUN pin may be externally pulled up or driven directly by logic. When driving the RUN pin with a low impedance source, do not exceed the absolute maximum rating of 6V. The RUN pin has an internal 6V voltage clamp that allows the RUN pin to be connected through a resistor to a higher voltage (for example, VIN), as long as the max- imum current into the RUN pin does not exceed 100μA. An external resistor divider connected to VIN can set the threshold for converter operation.

The start-up of the controller's output voltage VOUT is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.2V internal reference, the PL3900 regulates the VFB voltage to the SS pin voltage instead of the 1.2V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to SGND. An internal 10μA.pull-up current charges this capacitor creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V (and beyond up to INTVCC), the output voltage rises smoothly to its final value.

9.3 INTVCC/EXTVCC Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the INTVCC pin. When the EXTVCC pin is tied to a voltage less than 4.8V, the VBIAS LDO (low dropout linear regulator) supplies 5.4V from VBIAS to INTVCC. If EXTVCC is taken above 4.8V, the VBIAS LDO is turned off and an EXTVCC LDO is turned on. Once enabled, the EXTVCC LDO supplies 5.4V from EXTVCC to INTVCC. Using the EXTVCC pin allows the INTVCC power to be derived from an external source, thus removing the power dissipation of the VBIAS LDO.

9.4 Light Load Current Operation—Burst Mode Operation, Pulse-Skipping or Continuous Conduction PLLIN/MODE Pin

The PL3900 can be enabled to enter high efficiency Burst Mode operation, constant-frequency, pulse-skipping mode or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to SGND. To select forced continuous operation, tie the PLLIN/MODE pin to INTVCC. To select pulse-skipping mode, tie the PLLIN/ MODE pin to a DC voltage greater than 1.2V and less than INTVCC – 1.3V.

9.5 Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The switching frequency of the PL3900's controllers can be selected using the FREQ pin. If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to SGND, tied to INTVCC, or programmed through an external resistor. Tying FREQ to SGND selects 350kHz while tying FREQ to INTVCC selects 535kHz. Placing a resistor between FREQ and SGND allows the frequency to be programmed between 50kHz and 900kHz.

A phase-locked loop (PLL) is available on the PL3900 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The typical capture range of the PL3900's PLL is from approximately 55kHz to 1MHz, and is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 0.4V (falling).

9.6 Multi-Phase Applications (CLKOUT and PHASMD Pins)

The PL3900 features two pins, CLKOUT and PHASMD, which allow other controller ICs to be daisy-chained with the PL3900 in Multi-Phase applications. The clock output signal on the CLKOUT pin can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or multiple separate outputs. The PHASMD pin is used to adjust the phase of the CLKOUT signal as well as the relative phases between the two internal controllers, as summarized in Table 1. The phases are calculated relative to the zero degrees phase being defined as the rising edge of the bottom gate driver output of controller 1 (BG1). Depending on the phase selection, a Multi-Phase application with multiple PL3900s can be configured for 2-, 3-, 4- , 6- and 12-phase operation.

Table 1.

VPHASMD	CONTROLLER 2 PHASE (°C)	CLKOUT PHASE (°C)
GND	180	60
Floating	180	90
INTVCC	240	120

CLKOUT is disabled when the controller is in shutdown or in sleep mode.

9.7 Power Good

The PGOOD pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the VFB pin voltage is not within ±10% of the 1.2V reference voltage. The PGOOD pin is also pulled low when the corresponding RUN pin is low (shut down). When the VFB pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V (abs max).

9.8 BOOST Supply Refresh and Internal Charge Pump

Each top MOSFET driver is biased from the floating boot- strap capacitor, CB, which normally recharges during each cycle through an external diode when the bottom MOSFET turns on. There are two considerations for keeping the BOOST supply at the required bias level. During start-up, if the bottom MOSFET is not turned on within 100μs after UVLO goes low, the bottom MOSFET will be forced to turn on for ~400ns. This forced refresh generates enough

BOOST-SW voltage to allow the top MOSFET ready to be fully enhanced instead of waiting for the initial few cycles to charge up. There is also an internal charge pump that keeps the required bias on BOOST. The charge pump always operates in both forced continuous mode and pulse-skipping mode. In Burst Mode operation, the charge pump is turned off during sleep and enabled when the chip wakes up. The internal charge pump can normally supply a charging current of 55μA.

9.9 Current Comparator Sense Voltage Range setting (ILIM Pin)

This pin is used to set the peak current sense voltage in the current comparator. Connect this pin to INTVCC to set the peak current sense voltage to 60mV and the controller operates in constant voltage mode, Short circuit protection for hiccups can be achieved in buck mode. Connect this pin to SGND by a resistor to set the current sense voltage range and the controller operates in constant voltage and constant current mode.

9.10 Thermal Protection

The PL3900 includes an internal junction temperature monitor to protect the device in the event of a higher than normal junction temperature. If the junction temperature exceeds 150°C (typical), thermal shutdown occurs to prevent further power dissipation and temperature rise. The PL3900 initiates a restart sequence when the junction temperature falls to 135°C, based on a typical thermal shutdown hysteresis of 15°C. This is a non-latching protection, and, as such, the device cycles into and out of thermal shutdown if the fault persists.

9.11 Functional Block Diagram

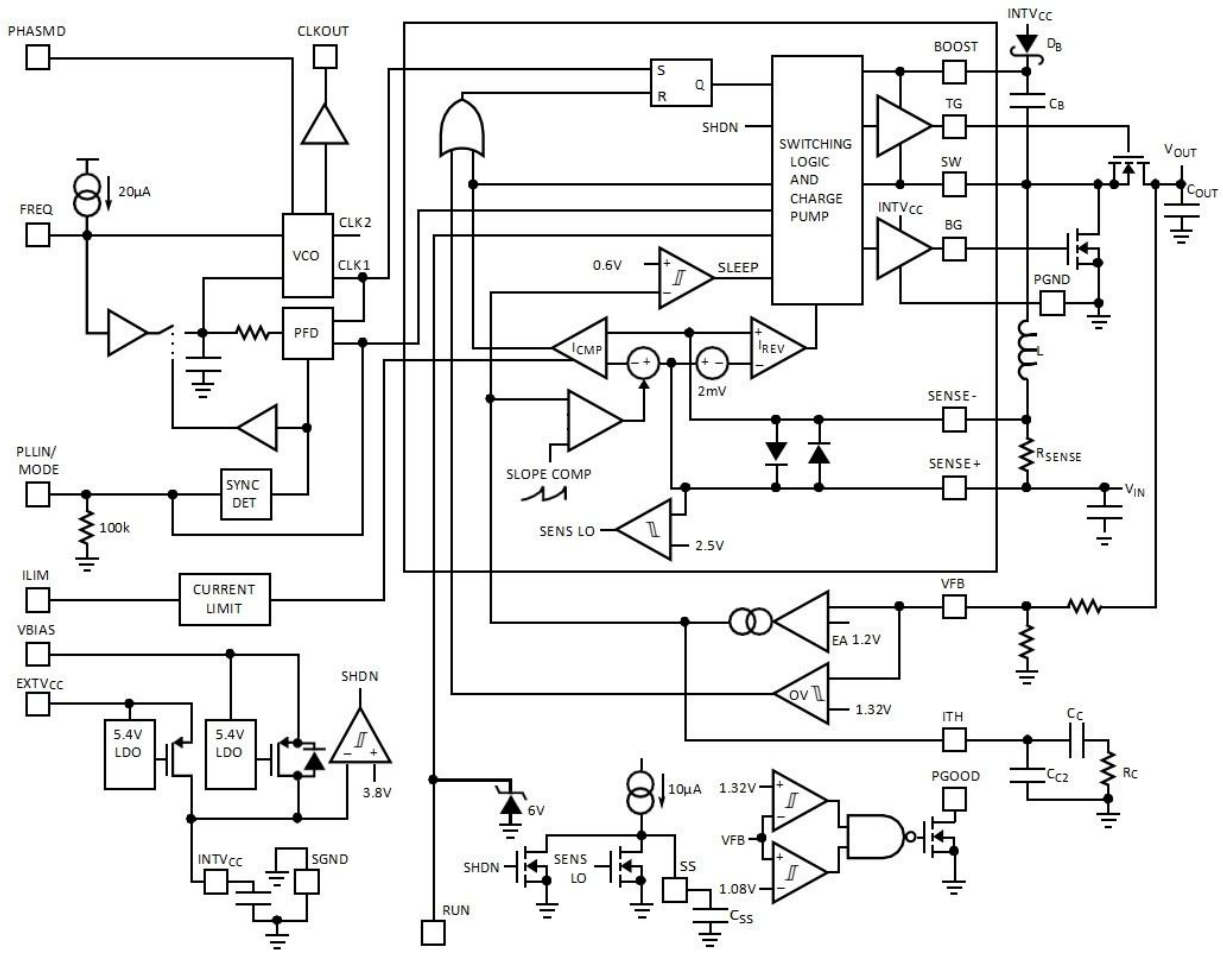


Fig9.11 Block Diagram

10 Applications and Implementation

10.1 Sense Resistor Current Sensing

RSENSE is chosen based on the required output current. The current comparator has a maximum threshold VSENSE(-MAX). When the ILIM pin is tied to INTVCC, the maximum threshold is set to 60mV. The current comparator threshold sets the peak of the inductor current, yielding a maximum average inductor current, IMAX, equal to the peak value less half the peak-to-peak ripple current, ΔIL. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

When this pin is tied a resistor to SGND , The peak current is determined as follows:

$$V_{SNS}(mV) = \frac{0.6 \times R_{Ilim}(k\Omega)}{1.5}$$

Where V_{SNS} Max must not exceed 60mV.

$$I_{MAX}(A) = \frac{2 \times V_{SNS}(mV)}{R_{SNS}(m\,\Omega)}$$

10.2 Setting the Output Voltage

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light load, it is

desirable to choose large resistance values for both R1 and R2. A value between 10k and1M is recommended for both resistors. If R1=100k is chosen, then R2 can be calculated to be:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right)$$

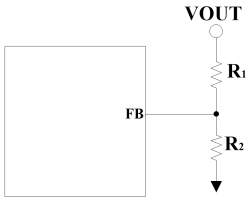


Fig 10.2 Setting Output Voltage

10.3 Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. Why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge and switching losses. Also, at higher frequency the duty cycle of body diode conduction is higher, which results in lower efficiency. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

For a given ripple, the inductance terms in continuous mode are as follows:

$$L_{BOOST} > \frac{V_{IN(MIN)}{}^2 * (V_{OUT} - V_{IN(MIN)}) * 1000}{f * \Delta I_L * V_{OUT}{}^2} uH$$

$$L_{BUCK} > \frac{V_{OUT} * (V_{IN(MAX)} - V_{OUT}) * 1000}{f * \Delta I_L * V_{IN(MAX)}} uH$$

where: f is operating frequency, kHz

VIN(MIN) is minimum input voltage, V

VIN(MAX) is maximum input voltage, V

VOUT is output voltage, V

ΔIL is maximum inductor ripple current, A, usually select 20~40% maximum current.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by RSENSE. Lower inductor values (higher ΔIL) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease. Once the value of L is known, an inductor with low DCR and low core losses should be selected.

10.4 Power MOSFET Selection

Two external power MOSFETs must be selected for each controller in the PL3900: one N-channel MOSFET for the main switch, and one N-channel MOSFET for the synchronous switch.

The peak-to-peak gate drive levels are set by the INTVCC voltage. This voltage is typically 5.4V during start up (see EXTVCC pin connection). Consequently, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the BVDSS specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance RDS(ON), Miller capacitance CMILLER, input voltage and maximum output current. In boost mode, When the IC is operating in continuous mode, the duty cycles for the main and synchronous MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}}$$

If the maximum output current is IOUT(MAX) and each channel takes one half of the total output current, the MOSFET power dissipations in each channel at maximum output current are given by:

$$P_{MAIN} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^2} \bullet \left(\frac{I_{OUT(MAX)}}{2}\right)^2 \bullet (1+\delta) \bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{OUT(MAX)}}{2 \bullet V_{IN}} \bullet C_{MILLER} \bullet f$$

$$P_{SYNC} = \frac{V_{IN}}{V_{OUT}} \bullet \left(\frac{I_{OUT(MAX)}}{2}\right)^2 \bullet (1+\delta) \bullet R_{DS(ON)}$$

Where d is the temperature dependency of RDS(ON) (approximately 1Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

10.5 CIN and COUT Selection

In the boost region, input current is continuous. In the buck region, input current is discontinuous. In the buck region, the selection of input capacitor CIN is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

$$I_{CIN} = I_{OUT(MAX)} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

This input current has a maximum at VIN = 2VOUT, ICIN(MAX) = IOUT(MAX)/2.

In the boost region, COUT must be capable of reducing the output voltage ripple because of the discontinuous output current. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{(BOOST,Cap)} = \frac{I_{OUT(MAX)} * (V_{OUT} - V_{IN(MIN)})}{C_{OUT} * V_{OUT} * f} V$$

where COUT is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{(BOOST,ESR)} = I_{OUT(MAX,BOOST)} * ESR$$

In buck mode, VOUT ripple is given by:

$$\Delta V_{OUT} \le \Delta I_L * \left(ESR + \frac{1}{8 * f * C_{OUT}}\right)$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

10.6 Multi-Phase Operation

For output loads that demand high current, multiple PL3900 s can be cascaded to run out-of-phase to provide more output current and at the same time to reduce input and output voltage ripple. The PLLIN/MODE pin allows the PL3900 to synchronize to the CLKOUT signal of another PL3900. The CLKOUT signal can be connected to the PLLIN/MODE pin of the following PL3900 stage to line up both the frequency and the phase of the entire system.

Tying the PHASMD pin to INTVCC, SGND or floating generates a phase difference (between PLLIN/MODE and CLKOUT) of 240°, 60° or 90°, respectively, and a phase difference (between CH1 and CH2) of 120°, 180°,or 180°. Figure 10.7 shows the connections necessary for 3-, 4-, 6- or 12-phase operation. A total of 12 phases can be cascaded to run

simultaneously out-of-phase with respect to each other.

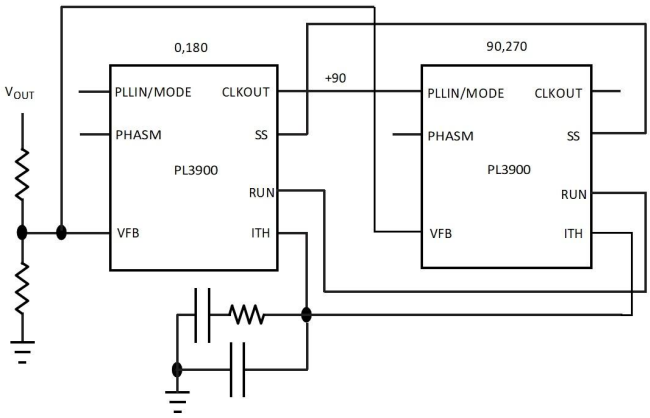


Fig10.6 4-Phase Operation

10.7 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during each cycle's turn-on and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1μF to 1μF. CBST should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1μF was selected for this design example.

10.8 Minimum On-Time Considerations

Minimum on-time, tON(MIN), is the smallest time duration that the PL3900 is capable of turning on the bottom MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET.

In forced continuous mode, if the input voltage is close to the output voltage , the controller will begin to skip cycles but the output will continue to be regulated. The minimum on-time for the PL3900 is approximately 110ns.

10.9 PCB Board Layout

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

Check the following in your layout:

1. The signal and power grounds must be separate. The combined IC signal ground pin and the ground return of CINTVCC must return to the combined COUT (–) terminals. The path formed by the top N-channel MOSFET, Schottky diode and the CIN capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.

2. Keep the SW, TG, and BOOST nodes away from sensitive small-signal nodes. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the PL3900 and occupy minimum PC trace area.

3. The INTVCC decoupling capacitor must be connected close to the IC, between the INTVCC and the power ground pins. This capacitor carries the MOSFET drivers' current peaks

4. The SENSE- and SENSE+ leads must be routed together with minimum PC trace spacing. The filter capacitor between SENSE+ and SENSE- should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.

5. The PL3900 VFB pin's resistive divider must be connected between the (+) terminal of COUT and signal ground. Great care should be taken to route the VFB line away from noise sources, such as the inductor or the SW line. Also keep the VFB node as small as possible to avoid noise pickup.

11 Application Examples

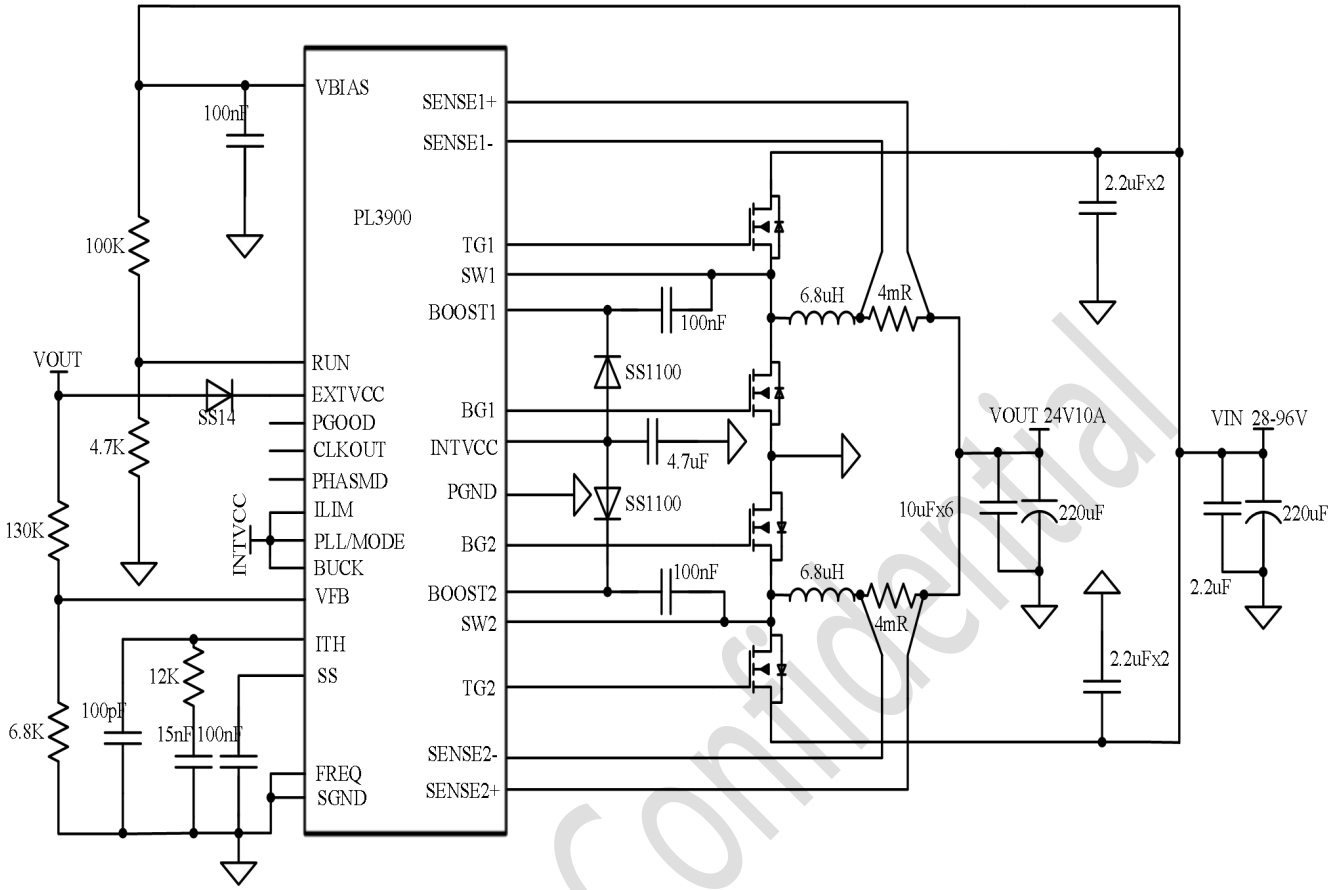


Fig11.1.1 High Efficiency 2-Phase 24V Buck Converter

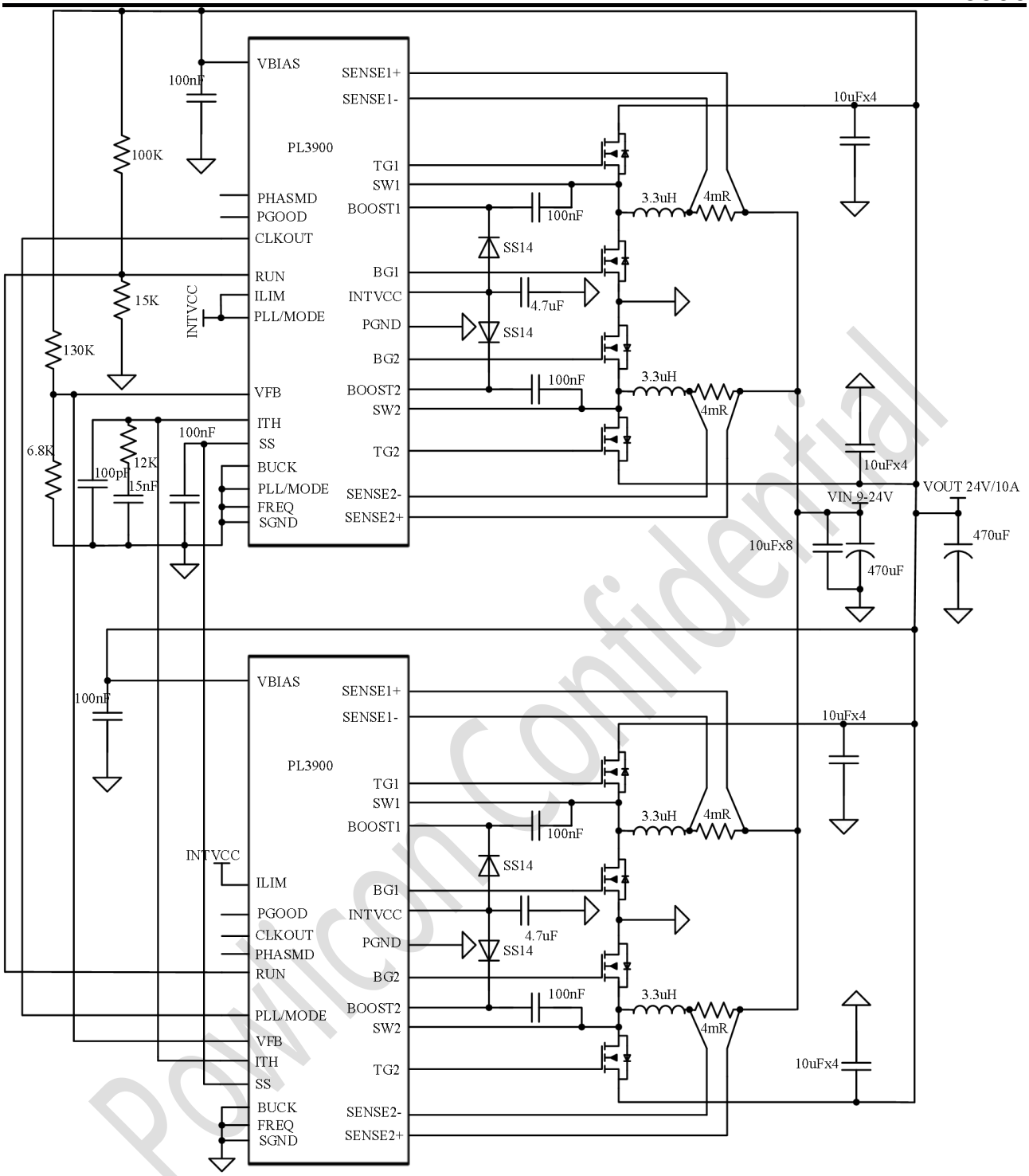


Fig11.1.2 4-Phase Single Output Boost Converter

11.2 Application Examples

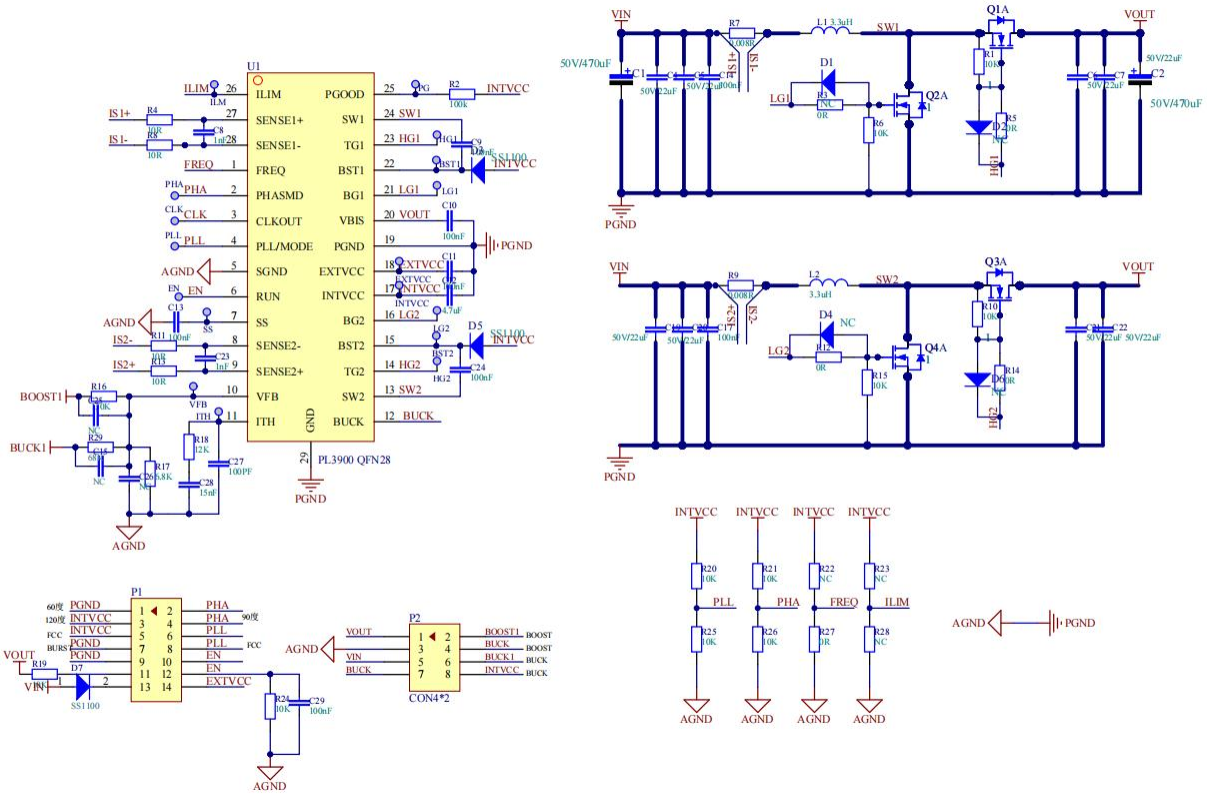


Fig11.2-1 Schematic

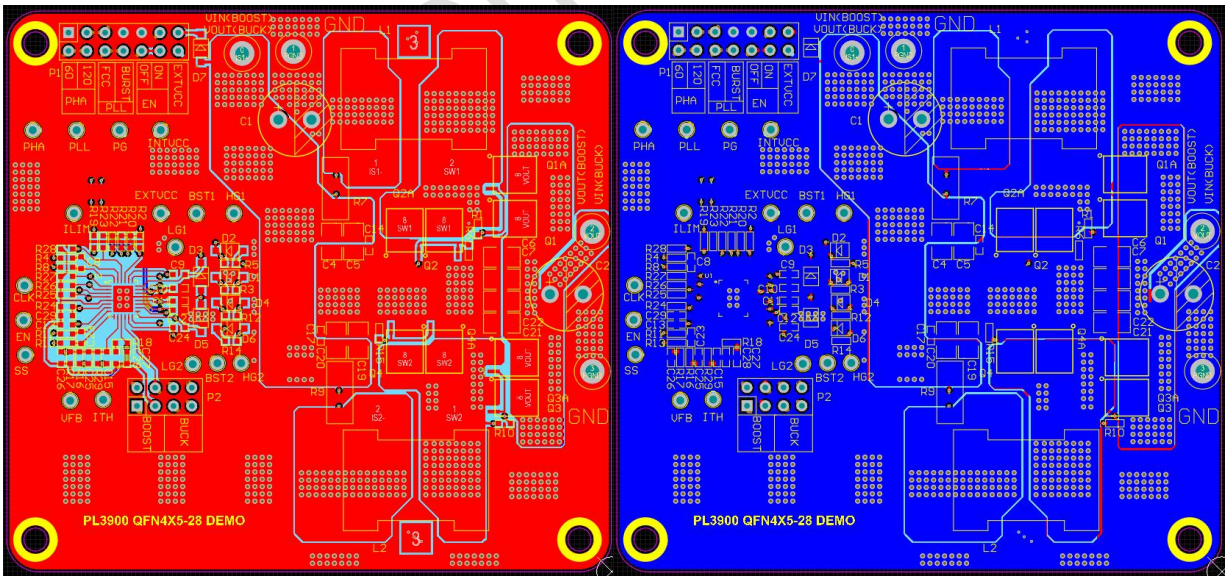
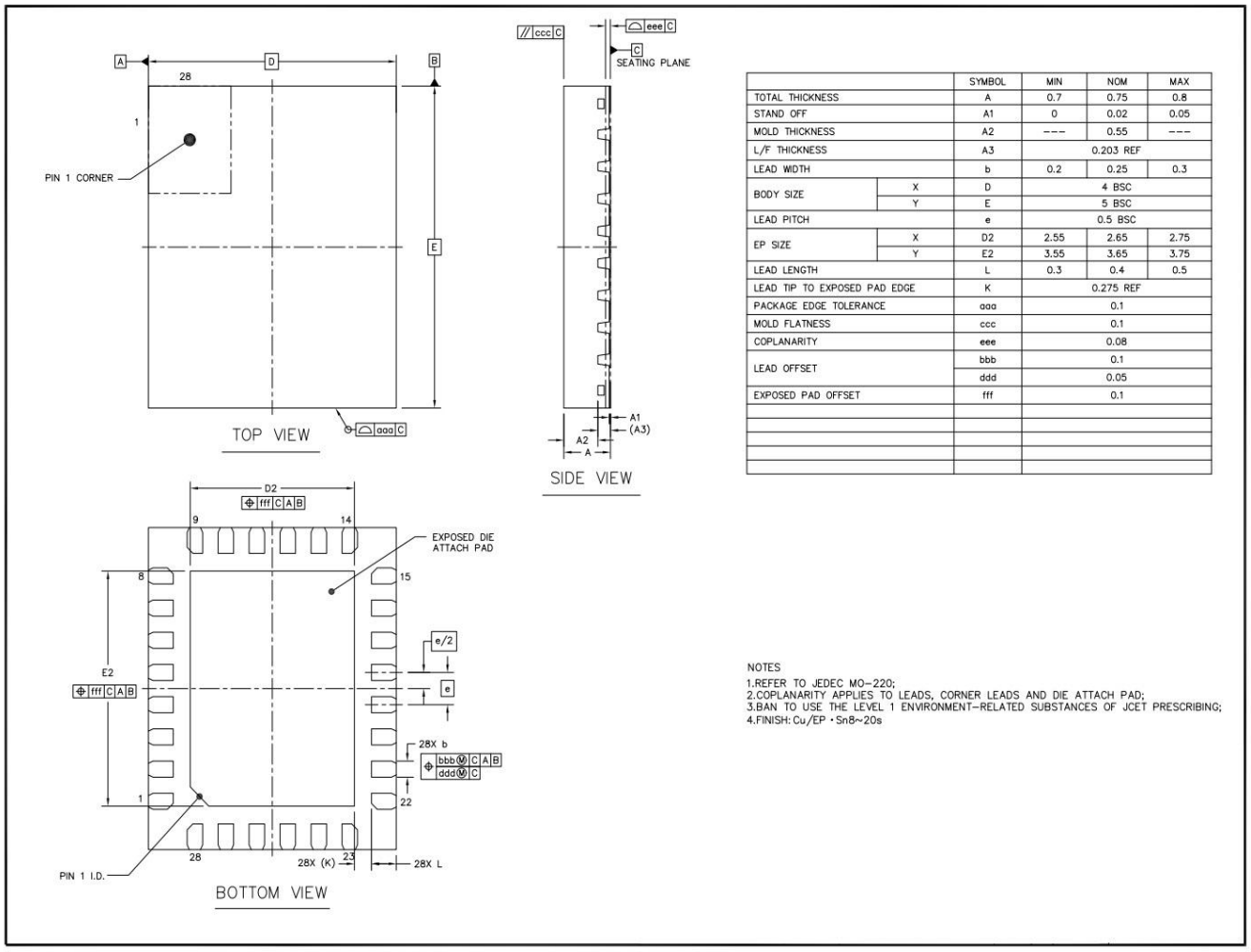


Fig11.2-2 PCB

12 Packaging Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	2.55	2.65	2.75
	Y	E2	3.55	3.65	3.75
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.275 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP · Sn8~20s