PL3901 100V Synchronous Buck/Boost Controller

1 Features

- Wide VIN Range:4.5V to 56V (Sense Pin 60V Abs Max) in Boost mode and Operates Down to 2.5V After Start-Up ， 4.5V to 96V (Vbias Pin 100V Abs Max) in Buck mode
- Output Voltage Up to 56V(Buck mode) and 96V(Boost mode)
- ±1% 1.200V Reference Voltage
- RSENSE or Inductor DCR Current Sensing
- Synchronous Operation for Highest Efficiency and Reduced Heat Dissipation
- 100% Duty Cycle Capability for Synchronous MOSFET in Boost Mode
- CV/CC Mode control (Constant voltage and constant current)
- Low Quiescent Current: 350μA
- Phase-Lockable Frequency (75kHz to 850kHz).
- Programmable Fixed Frequency (50kHz to 900kHz)
- Power Good Output Voltage Monitor
- Low Shutdown Current, IQ < 8μA
- Internal LDO Powers Gate Drive from VBIAS or EXTVCC
- Thermally Enhanced Low Profile 20-Pin 3mm × 4mm QFN Package

2 Applications

- consumer
- Industrial
- Automotive
- Medical

3 Description

The PL3901 is a high performance synchronous buck/boost converter controller . Synchronous rectification in creases efficiency, reduces power losses and eases thermal requirements, enabling high power boost applications.

A 4.5V to 56V (boost mode) and 4.5V to 96V (buck mode) input supply range encompasses a wide range of system architectures and battery chemistries. In boost mode,When biased from the output of the converter or another auxiliary supply, the PL3901 can operate from an input supply as low as 2.5V after start-up. The operat ing frequency can be set for a 50kHz to 900kHz range or synchronized to an external clock using the internal PLL.

The TRACK/SS pin ramps the output voltage during start-up. The PLLIN/MODE pin selects Burst Mode operation, pulse skipping mode or forced continuous mode at light loads.

4 Typical Application Schematic

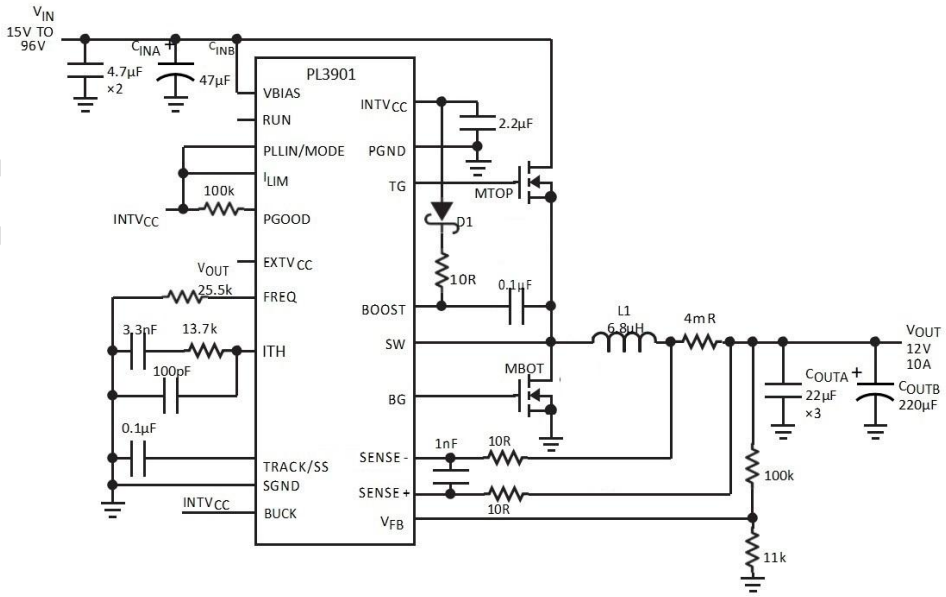
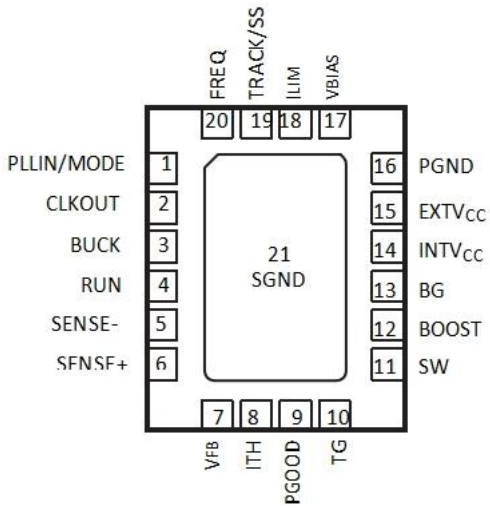


Fig4.1 Typical Application Schematic

5 Pin Configuration and Functions



UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN

Fig5-1 Pin-Function

Pin		Description
Number	Name	
1	PLLIN/MODE	External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, it will force the controller into forced continuous mode of operation and the phase-locked loop will force the rising BG1 signal to be synchronized with the rising edge of the external clock. When not synchronizing to an external clock, this input determines how the PL3901 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to INTVCC forces continuous inductor current operation. Tying this pin to a voltage greater than 1.2V and less than INTVCC-1.3V selects pulse-skipping operation. This can be done by adding a 100k resistor between the PLLIN/ MODE pin and INTVCC.
2	CLKOUT	Logic output that provides a clock signal that is 180° out-of-phase with the high-side FET gate drive.
3	BUCK	This pin connect to Ground or Float to set PL3901 in Boost mode. This pin connect Intvcc pin to set PL3901 in buck mode.
4	RUN	Run Control Input. Forcing this pin below 1V shuts down the entire PL3901, An external resistor divider connected to VIN can set the threshold for converter operation.
5	SENSE–	Nega-tive Current Sense Comparator Input. The (–) input to the current comparator is normally connected to the negative terminal of a current sense resistor connected in series with the inductor.
6	SENSE+	Positive Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the positive terminal of a current sense resistor. The current sense resistor is normally placed at the input of the boost controller and the output of the buck controller in series with the inductor. This pin also supplies power to the current comparator. The common mode voltage range on SENSE+ and SENSE – pins is 2.5V to 56V (60V abs max).
7	VFB	Error Amplifier Feedback Input. This pin receives the remotely sensed feedback voltage from an external resistive divider connected across the output.
8	ITH	Current Control Threshold and Error Amplifier Compensation Point. The voltage on this pin sets the current trip threshold.
9	PGOOD	Power Good Indicator. Opendrain logic output that is pulled to ground when the output voltage is more than ±10 % away from the regulated output voltage. To avoid false trips the output voltage must be outside the range for 25μs before this output is activated.
10	TG	Top Gate. Connect to the gate of the synchronous N-channel MOSFET.

11	SW	Switch Node. Connect to the source of the synchronous N-channel MOSFET, the drain of the main N-channel MOSFET and the inductor.
12	BOOST	Floating power supply for the synchronous N-channel MOSFET,Bypass to SW with a capacitor and supply with a Schottky diode connected to INTVCC.
13	BG	Bottom Gate. Connect to the gate of the main N-channel MOSFET.
14	INTVCC	Output of Internal 5.4V LDO. Power supply for control circuits and gate drivers. De-couple this pin to GND with a minimum 4.7μF low ESR ceramic capacitor.
15	EXTVCC	External Power Input. When this pin is between 4.8V and 30V, an internal switch bypasses the internal regulator and supply power to INTVCC directly from EXTVCC. Do not float this pin. It can be connected to ground when not used.
16	PGND	Driver Power Ground. Connects to the sources of bottom (main) N-channel MOSFETs and the (–) terminal(s) of CIN and COUT.
17	VBIAS	Main Supply Pin. It is normally tied to the input supply VIN or to the output of the boost converter. A bypass capacitor should be tied between this pin and the signal ground pin. The operating voltage range on this pin is 4.5V to 96V (100V abs max).
18	ILIM	Current Comparator Sense Voltage Range setting. This pin is used to set the peak current sense voltage in the current comparator. Connect this pin to INTVCC to set the peak current sense voltage to 60mV and the controller operates in constant voltage mode,Short circuit protection for hiccups can be achieved in buck mode. Connect this pin to SGND by a resistor to set the current sense voltage range and the controller operates in constant voltage and constant current mode.
19	TRACK/SS	External Tracking and Soft-Start Input. The PL3901 regulates the VFB voltage to the smaller of 1.2V or the voltage on the TRACK/SS pin. An internal 10μA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. Alternatively, a resistor divider on another voltage supply connected to this pin allows the PL3901 output to track another supply during start-up.
20	FREQ	Frequency Control Pin for the Internal VCO. Connecting the pin to SGND forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to INTVCC forces the VCO to a fixed high frequency of 535kHz. The frequency can be programmed from 50kHz to 900kHz by connecting a resistor from the FREQ pin to SGND. The resistor and an internal 20μA source current create a voltage used by the internal oscillator to set the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.
21	SGND	Signal ground，Exposed pad of the package and connect to a large copper plane to reduce thermal resistance.

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL3901	**PL3901IQN20A**	**QFN3X4-20L**	**4000**	**3901 RAAYMD**

3901: Part Number
RAAYMD : RAA: LOT NO.; YMD: Package Date Code

7 Specifications

7.1 Absolute Maximum Ratings(Note1)

PARAMETER	MIN	MAX	Unit
VBIAS to GND	-0.3	100	V
BOOST to GND	-0.3	100	
SW to GND	-0.3	100	
RUN to GND	-0.3	6	
PGOOD, PLLIN/MODE to GND	-0.3	6	
INTVCC to GND, (BOOST- SW)	-0.3	6	
EXTVCC to GND	-0.3	30	
SENSE+, SENSE－ to GND	-0.3	60	
SENSE+ ----SENSE－	-0.3	0.3	
ILIM, SS, ITH, FREQ, SS, VFB to GND	-0.3	6	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
TST	Storage Temperature Range	-65	150	°C
TJ	Junction Temperature	-40	+150	°C
VESD	HBM Human body model	2		kV

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
VBIAS Voltages	VBIAS	5.0	100	V
Temperature	Operating junction temperature range, TJ	-40	+150	°C

7.4 Thermal Information(Note 3)

Symbol	Description	QFN3X4-20L	Unit
θJA	Junction to ambient thermal resistance	53	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

7.5 Electrical Characteristics

The I denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at TA = 25°C, VBIAS = 12V, unless otherwise noted (Note 2).

Supply voltages	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VBIAS	Chip Bias Voltage Operating Range		4.5		100	V
VFB	Regulated Feedback Voltage	ITH = 1.2V (Note 4)	1.188	1.200	1.212	V
IFB	Feedback Current	(Note 4)		±5	±50	nA
VREFLNREG	Reference Line Voltage Regulation	VBIAS = 6V to 98V		0.002	0.02	%/V
VLOADREG	Output Voltage Load Regulation (Note 4)	Measured in Servo Loop; ΔITH Voltage = 1.2V to 0.7V		0.01	0.1	%
		Measured in Servo Loop; ΔITH Voltage = 1.2V to 2V		–0.01	–0.1	%
gm	Error Amplifier Transconductance	ITH = 1.2V	2			mmho
IQ	Input DC Supply Current Pulse-Skipping or Forced Continuous Mode	(Note 5) RUN = 5V; VFB = 1.25V (No Load)		1.2		mA
	Sleep Mode	RUN = 5V; VFB = 1.25V (No Load)		350	500	μA
	Shutdown	RUN = 0V		8	20	μA
UVLO	INTVCC Undervoltage Lockout Thresholds	VINTVCC Ramping Up VINTVCC Ramping Down	 3.6	4.1 3.8	4.3	V V
VRUN	RUN Pin ON Threshold	VRUN Rising	1	1.2		V
VRUNHYS	RUN Pin Hysteresis		200			mV
ISS	Soft-Start Charge Current	VSS = GND	7	10	13	μA
VSENSE(MAX)	Maximum Current Sense Threshold	VFB = 1.1V, ILIM = INTVCC VFB = 1.1V, ILIM = GND		60 60		mV mV
VSENSE(CM)	SENSE Pins Common Mode Range	Boost mode Buck mode	2.5 0		60 60	V V
ISENSE+	SENSE+ Pin Current	VFB = 1.1V, ILIM = GND		200	300	μA
ISENSE–	SENSE– Pin Current	VFB = 1.1V, ILIM = GND			±1	μA
tr(TG)	Top Gate Rise Time	CLOAD = 3300pF (Note 6)		20		ns
tf(TG)	Top Gate Fall Time	CLOAD = 3300pF (Note 6)		20		ns
tr(BG)	Bottom Gate Rise Time	CLOAD = 3300pF (Note 6)		20		ns
tr(BG)	Bottom Gate Fall Time	CLOAD = 3300pF (Note 6)		20		ns
RUP(TG)	Top Gate Pull-Up Resistance			1.2		Ω
RDN(TG)	Top Gate Pull-Down Resistance			1.2		Ω
RUP(TG)	Bottom Gate Pull-Up Resistance			1.2		Ω
RDN(TG)	Bottom Gate Pull-Down Resistance			1.2		Ω
tD(TG/BG)	Top Gate Off to Bottom Gate On Switch-On Delay Time	CLOAD = 3300pF (Each Driver)		70		ns
tD(BG/TG)	Bottom Gate Off to Top Gate On Switch-On Delay Time	CLOAD = 3300pF (Each Driver)		70		ns

DMAX	Maximum Duty Cycle			96		%
tON(MIN)	Minimum On-Time	(Note 7)		110		ns
INTVCC Linear Regulator						
VINTVCC(VIN)	Internal VCC Voltage	6V < VBIAS < 56V, VEXTVCC = 0	5.2	5.4	5.6	V
VLDO INT	INTVCC Load Regulation	ICC = 0mA to 50mA	0.5	2		%
VINTVCC(EXT)	Internal VCC Voltage	VEXTVCC = 6V	5.2	5.4	5.6	V
VLDO EXT	INTVCC Load Regulation	ICC = 0mA to 40mA, VEXTVCC = 6V	0.5	2		%
VEXTVCC	EXTVCC Switchover Voltage	EXTVCC Ramping Positive	4.5	4.8	5	V
VLDOHYS	EXTVCC Hysteresis		250			mV
Oscillator and Phase-Locked Loop						
fPROG	Programmable Frequency	RFREQ = 25k RFREQ = 60k RFREQ = 100k	 335	105 400 760	 465	kHz kHz kHz
fLOW	Lowest Fixed Frequency	VFREQ = 0V	320	350	380	kHz
fHIGH	Highest Fixed Frequency	VFREQ = INTVCC	488	535	585	kHz
fSYNC	Synchronizable Frequency	PLLIN/MODE = External Clock	75		850	kHz
PGOOD Output						
IPGOOD	PGOOD Leakage Current	VPGOOD = 5V	±1			µA
VPGOOD	PGOOD Trip Level	VFB with Respect to Set Regulated Voltage VFB Ramping Negative Hysteresis	–12 2.5	-10	-8	 % %
		VFB Ramping Positive Hysteresis	8 2.5	10	12	% %
tPGOOD(DELAY)	PGOOD Delay	PGOOD Going High to Low	25			µs
BOOST Charge Pump						
IBOOST	BOOST Charge Pump Available Output Current	VSW= 12V; VBOOST– VSW= 4.5V; FREQ = 0V, Forced Continuous or Pulse-Skipping Mode	55			µA
THERMAL SHUTDOWN						
TSD	Thermal shutdown threshold	TJ rising	150			° C
TSD-HYS	Thermal shutdown hysteresis		15			° C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The PL3901 is tested under pulsed load conditions such that TJ ≈ TA. the PL3901 is guaranteed over the –40°C to 150°C operating temperature range . High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 150°C. Note that the maximum ambient temperature consistent with these

specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (TJ, in °C) is calculated from the ambienttemperature (TA, in °C) and power dissipation (PD, in Watts) according to the formula: TJ = TA + (PD • JA), where JA = 53°C/W for the QFN package .

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: The PL3901 is tested in a feedback loop that servos VFB to the output of the error amplifier while maintaining ITH at the midpoint of the current limit range.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: see Minimum On-Time Considerations in the Applications Information section.

8 Typical Characteristics

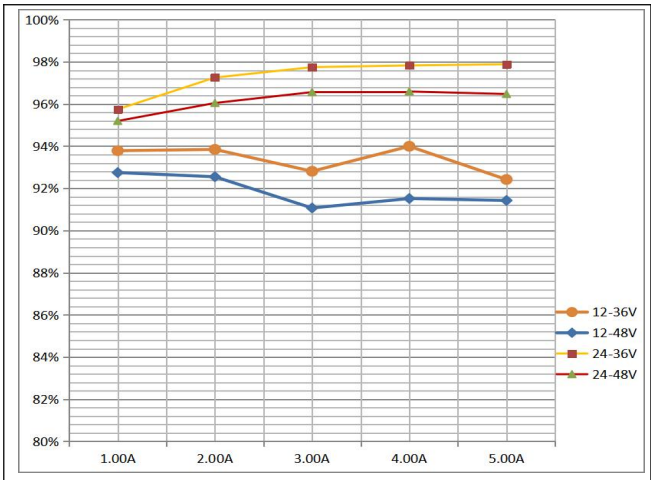


Fig8-1 Efficiency Boost Mode

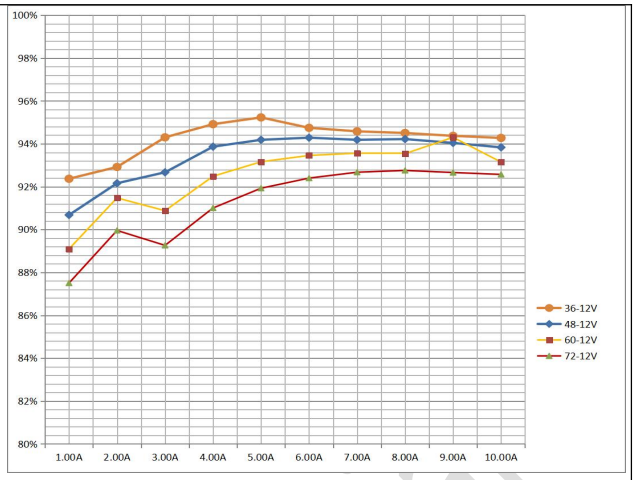
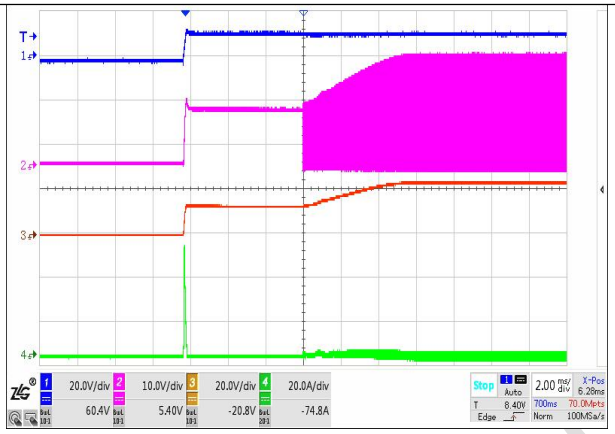
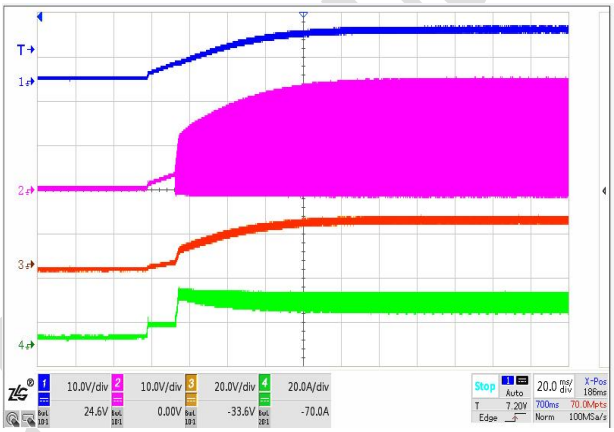


Fig8-2 Efficiency Buck Mode



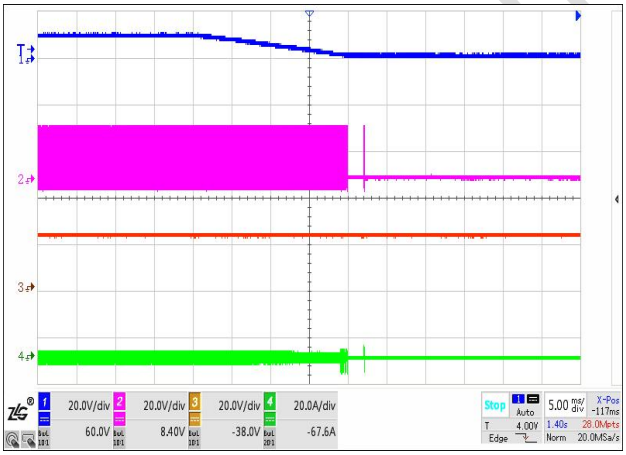
1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=12V Vout=24V

Fig8-3 Vin Start up waveform, Iout =0A,Boost Mode



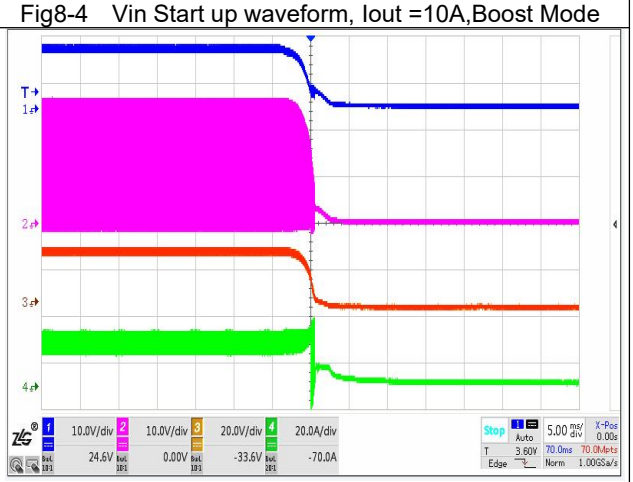
1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=12V Vout=24V

Fig8-4 Vin Start up waveform, Iout =10A,Boost Mode



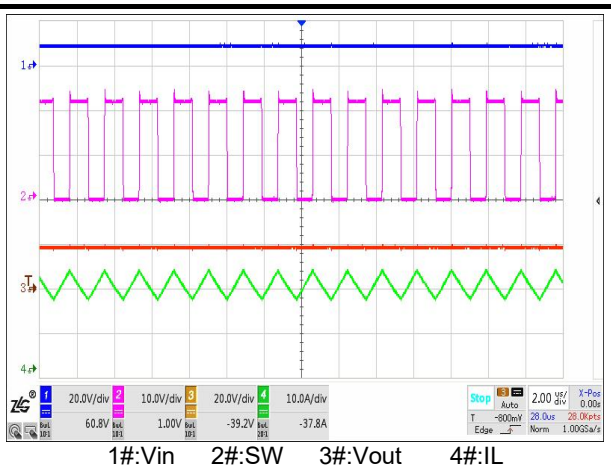
1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=12V Vout=24V

Fig8-5 Vin Shut down waveform, Iout =0A,Boost Mode

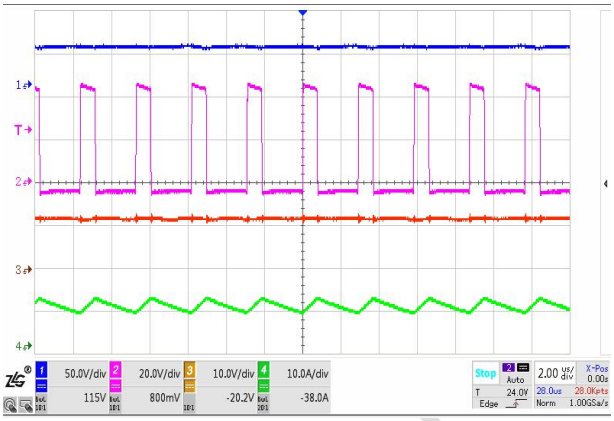


1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=12V Vout=24V

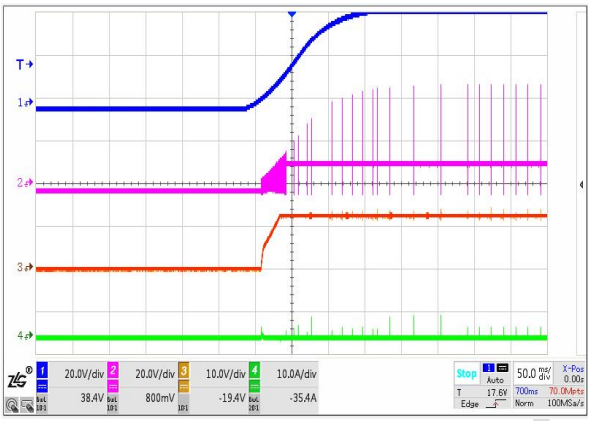
Fig8-6 Vin Shut down waveform, Iout =10A,Boost Mode



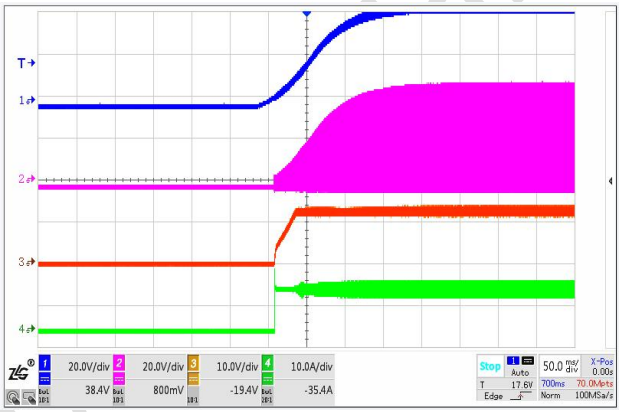
1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=12V Vout=24V
Fig8-7 Steady State waveform, Iout =10A,Boost Mode



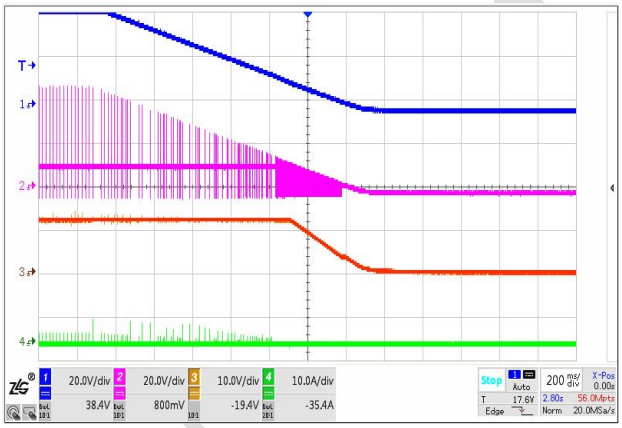
1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=48V Vout=12V
Fig8-8 Steady State waveform, Iout =10A,Buck Mode



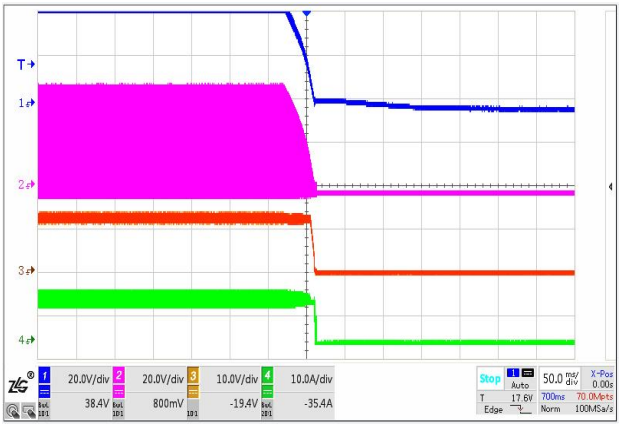
1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=48V Vout=12V
Fig8-9 Vin Start up waveform,Iout =0A,Buck Mode



1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=48V Vout=12V
Fig8-10 Vin Start up waveform, Iout =10A,Buck Mode



1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=48V Vout=12V
Fig8-11 Vin Shut down waveform, Iout =0A,Buck Mode



1#:Vin 2#:SW 3#:Vout 4#:IL
Vin=48V Vout=12V
Fig8-12 Vin Shut down waveform, Iout =10A,Buck Mode

9 Detailed Descriptions

9.1Main Control Loop

The PL3901 uses a constant-frequency, current mode step-up and step-down architecture . During normal operation, the external top MOSFET is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier EA. The error amplifier compares the output voltage feedback signal at the VFB pin (which is generated with an external resistor divider connected across the output voltage, VOUT, to ground), to the internal 1.200V reference voltage. In a boost converter, the required inductor current is determined by the load current, VIN and VOUT. When the load current increases, it causes a slight decrease in VFB relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current in each channel matches the new requirement based on the new load current.

After the bottom MOSFET is turned off each cycle, the top MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator, IR, or the beginning of the next clock cycle.

9.2 INTVCC/EXTVCC Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the INTVCC pin. When the EXTVCC pin is tied to a voltage less than 4.8V, the VBIAS LDO (low dropout linear regulator) supplies 5.4V from VBIAS to INTVCC. If EXTVCC is taken above 4.8V, the VBIAS LDO is turned off and an EXTVCC LDO is turned on. Once enabled, the EXTVCC LDO supplies 5.4V from EXTVCC to INTVCC. Using the EXTVCC pin allows the INTVCC power to be derived from an external source, thus removing the power dissipation of the VBIAS LDO.

9.3 Shutdown and Start-Up (RUN and TRACK/SS Pins)

The internal controllers of the PL3901 can be shut down using the RUN pin. Pulling this pin below 1V disables both controllers and most internal circuits, including the INTVCC LDOs. In this state, the PL3901 draws only 8μA of quiescent current.

NOTE: Do not apply a heavy load for an extended time while the chip is in shutdown. The top MOSFETs will be turned off during shutdown and the output load may cause excessive dissipation in the body diodes.

The RUN pin may be externally pulled up or driven directly by logic. When driving the RUN pin with a low impedance source, do not exceed the absolute maximum rating of 6V. The RUN pin has an internal 6V voltage clamp that allows the RUN pin to be connected through a resistor to a higher voltage (for example, VIN), as long as the max- imum current into the RUN pin does not exceed 100μA. An external resistor divider connected to VIN can set the threshold for converter operation.

The start-up of the controller's output voltage VOUT is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 1.2V internal reference, the PL3901 regulates the VFB voltage to the TRACK/SS pin voltage instead of the 1.2V reference. This allows the TRACK/SS pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS pin to SGND. An internal 10μA pull-up current charges this capacitor creating a voltage ramp on the TRACK/ SS pin. As the TRACK/SS voltage rises linearly from 0V to 1.2V (and beyond up to 5V), the output voltage VOUT rises smoothly from zero to its final value. Alternatively the TRACK/SS pin can be used to cause the start-up of VOUT to track that of another supply. Typically, this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground (see Applications Information section).

9.4 Light Load Current Operation—Burst Mode Operation, Pulse-Skipping or Continuous Conduction PLLIN/MODE Pin

The PL3901 can be enabled to enter high efficiency Burst Mode operation, constant-frequency, pulse-skipping mode or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to ground (e.g., SGND). To select forced continuous operation, tie the PLLIN/MODE pin to INTVCC. To select pulse-skipping mode, tie the PLLIN/ MODE pin to a DC voltage greater than 1.2V and less than INTVCC – 1.3V.

When the controller is enabled for Burst Mode opera- tion, the minimum peak current in the inductor is set to approximately 30% of the maximum sense voltage even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the required current, the error amplifier EA will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off.

In sleep mode much of the internal circuitry is turned off and the PL3901 draws only 350μA of quiescent current. In sleep mode the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low and the controller resumes normal operation by turning on the bottom external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse

current comparator (IR) turns off the top external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous current operation.

In forced continuous operation or when clocked by an external clock source to use the phase-locked loop (see the Frequency Selection and Phase-Locked Loop section), the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantages of lower output voltage ripple and less interference to audio circuitry, as it maintains constant-frequency operation independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode, the PL3901 operates in PWM pulse-skipping mode at light loads. In this mode, constant-frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator ICMP may remain tripped for several cycles and force the external bottom MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

9.5 Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching loss- es, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the PL3901's controllers can be selected using the FREQ pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to SGND, tied to INTVCC, or programmed through an external resistor. Tying FREQ to SGND selects 350kHz while tying FREQ to INTVCC selects 535kHz. Placing a resistor between FREQ and SGND

allows the frequency to be programmed between 50kHz and 900kHz.

A phase-locked loop (PLL) is available on the PL3901 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. the typical capture range of the PL3901's PLL is from approximately 55kHz to 1MHz, and is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 0.4V (falling).

9.6 Clock signal output (CLKOUT Pin)

Logic output that provides a clock signal that is 180° out-of-phase with the high-side FET gate drive. Connect CLKOUT of the master PL3901 to the PLL pin of a second PL3901 to operate two controllers at the same frequency with 180° interleaved high-side FET switch turn-on transitions.

CLKOUT is disabled when the controller is in shutdown or in sleep mode.

9.7 Operation When VIN > Regulated VOUT

When VIN rises above the regulated VOUT voltage, the boost controller can behave differently depending on the mode, inductor current and VIN voltage. In forced continuous mode, the loop works to keep the top MOSFET on con- tinuously once VIN rises above VOUT. The internal charge pump delivers current to the boost capacitor to maintain a sufficiently high TG voltage.

In pulse-skipping mode, if VIN is between 100% and 110% of the regulated VOUT voltage, TG turns on if the inductor current rises above a certain threshold and turns off if the inductor current falls below this threshold. This threshold current is set to approximately 6% or 3% of the maximum ILIM current when the ILIM pin is grounded or tied to INTVCC, respectively. If the controller is programmed to Burst Mode operation under this same VIN window, then TG remains off regardless of the inductor current.

If VIN rises above 110% of the regulated VOUT voltage in any mode, the controller turns on TG regardless of the inductor current. In Burst Mode operation, however, the internal charge pump turns off if the chip is asleep. With the charge pump off, there would be nothing to prevent the boost capacitor from discharging, resulting in an insufficient TG voltage needed to keep the top MOSFET completely on. To prevent excessive power dissipation across the body diode of the top MOSFET in this situation, the chip can be switched over to forced continuous mode to enable the charge pump or a Schottky diode can also be placed in parallel to the top MOSFET.

9.8 Power Good

The PGOOD pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the VFB pin voltage is not within ±10% of the 1.2V reference voltage. The PGOOD pin is also pulled

low when the corresponding RUN pin PL3901 is low (shut down). When the VFB pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V (abs max).

9.9 Operation at Low SENSE Pin Common Mode Voltage

The current comparator in the is powered directly from the SENSE+ pin. In boost mode this enables the common mode voltage of the SENSE+ and SENSE– pins to operate at as low as 2.5V, which is below the UVLO threshold. The figure on the first page shows a typical application in which the controller's VBIAS is powered from VOUT while the VIN supply can go as low as 2.5V. If the voltage on SENSE+ drops below 2.5V, the SS pin will be held low. When the SENSE voltage returns to the normal operating range, the SS pin will be released, initiating a new soft-start cycle.

9.10 BOOST Supply Refresh and Internal Charge Pump

Each top MOSFET driver is biased from the floating boot- strap capacitor, CB, which normally recharges during each cycle through an external diode when the bottom MOSFET turns on. There are two considerations for keeping the BOOST supply at the required bias level. During start-up, if the bottom MOSFET is not turned on within 100µs after UVLO goes low, the bottom MOSFET will be forced to turn on for ~400ns. This forced refresh generates enough

BOOST-SW voltage to allow the top MOSFET ready to be fully enhanced instead of waiting for the initial few cycles to charge up. There is also an internal charge pump that keeps the required bias on BOOST. The charge pump always operates in both forced continuous mode and pulse-skipping mode. In Burst Mode operation, the charge pump is turned off during sleep and enabled when the chip wakes up. The internal charge pump can normally supply a charging current of 55µA.

9.11 Current Comparator Sense Voltage Range setting (ILIM Pin)

This pin is used to set the peak current sense voltage in the current comparator. Connect this pin to INTVCC to set the peak current sense voltage to 60mV and the controller operates in constant voltage mode,Short circuit protection for hiccups can be achieved in buck mode. Connect this pin to SGND by a resistor to set the current sense voltage range and the controller operates in constant voltage and constant current mode.

9.12 Functional Block Diagram

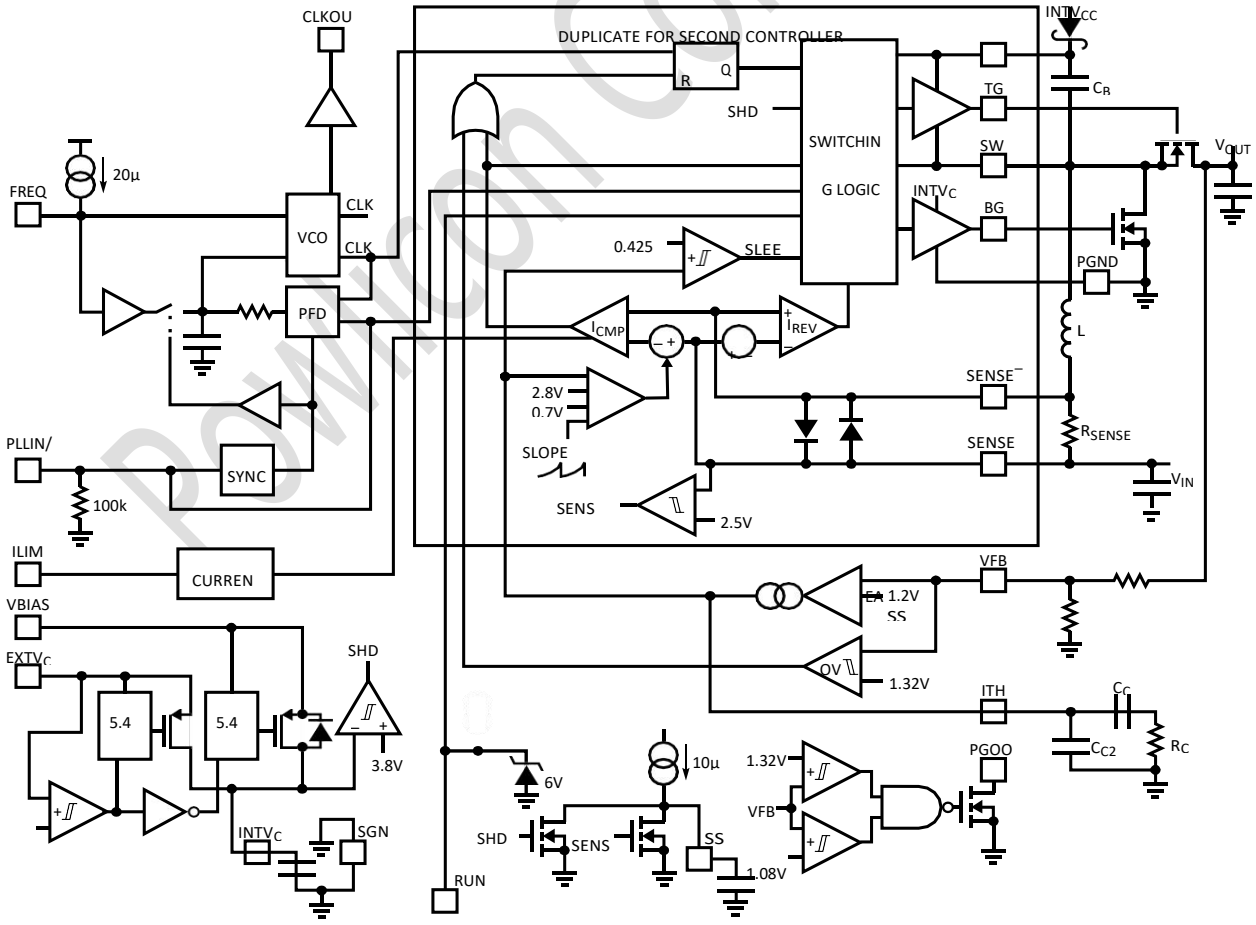


Fig9-12 Block Diagram

9.13 Thermal Protection

The PL3901 includes an internal junction temperature monitor to protect the device in the event of a higher than normal junction temperature. If the junction temperature exceeds 150°C (typical), thermal shutdown occurs to prevent further power dissipation and temperature rise. The PL3901 initiates a restart sequence when the junction temperature falls to 135°C, based on a typical thermal shutdown hysteresis of 15°C. This is a nonlatching protection, and, as such, the device cycles into and out of thermal shutdown if the fault persists.

10 Applications and Implementation

The Typical Application on the first page is a basic PL3901 application circuit.PL3901 can be configured to use either inductor DCR (DC resistance) sensing or a discrete sense resistor (RSENSE) for current sensing. The choice between the two current sensing schemes is largely a design trade- off between cost, power consumption and accuracy. DCR sensing is becoming popular because it does not require current sensing resistors and is more power-efficient,especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the se- lection of RSENSE (if RSENSE is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected.

10.1 SENSE+ and SENSE－Pins

The SENSE+ and SENSE－ pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 2.5V to 56V in boost mode. The current sense resistor is normally placed at the input of the boost controller and the output of the buck controller in series with the inductor.

The SENSE+ pin also provides power to the current com- parator. It draws ~200μA during normal operation. There is a small base current of less than 1μA that flows into the SENSE－ pin. The high impedance SENSE－ input to the current comparators allows accurate DCR sensing.

Filter components mutual to the sense lines should be placed close to the PL3901, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Fig 10.1.1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Fig b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

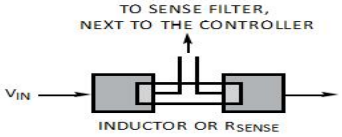
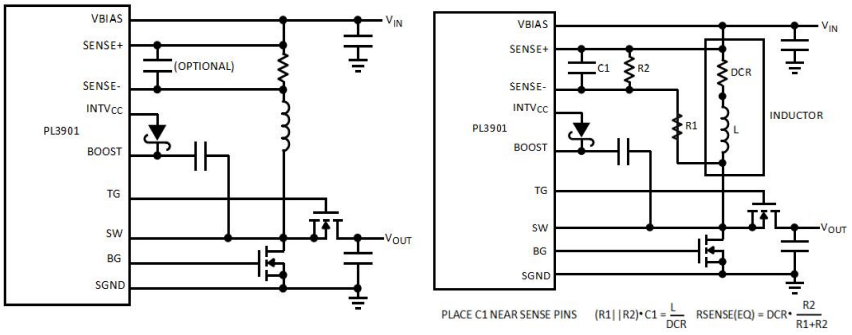


Fig 10.1.1 Sense Lines Placement with Inductor or Sense Resistor



(a) Using a Resistor to Sense Current **(b) Using the Inductor DCR to Sense Current**

Fig 10.1.2 Two Different Methods of Sensing Current

10.2 Sense Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Fig10.1.2-a. RSENSE is chosen based on the required output current.

The current comparator has a maximum threshold VSENSE(- MAX). When the ILIM pin is tied to INTVCC, the maximum threshold is set to 60mV. The current comparator threshold sets the peak of the inductor current, yielding a maximum average inductor current, IMAX, equal to the peak value less half the peak-to-peak ripple current, ΔIL. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

When this pin is tied a resistor to SGND ,The peak current is determined as follows:

$$V_{SNS}(mV) = \frac{0.6 \times R_{Ilim}(k\Omega)}{1.5}$$

Where V_{SNS} Max must not exceed 60mV.

$$I_{MAX}(A) = \frac{V_{SNS}(mV)}{R_{SNS}(m\,\Omega)}$$

10.3 Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the PL3901 is capable of sensing the voltage drop across the inductor DCR, as shown in Fig10.1.2-b. The DCR of the inductor can be less than 1mΩ for high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor could reduce the efficiency by a few percent compared to DCR sensing.

If the external R1||R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature. Consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the induct- or value calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the maximum current sense threshold (VSENSE(MAX)).

Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for the maximum inductor temperature (TL(MAX)) is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX}\ at\ T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1μF to 0.47μF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the SENSE– pin's ±1μA current.

The equivalent resistance R1|| R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR\ at\ 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D};\quad R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, at boost mode,will occur in continuous mode at VIN = 1/2VOUT:

$$P_{LOSS\_R1} = \frac{(V_{OUT} - V_{IN}) \bullet V_{IN}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

10.4 Inductor Value Calculation

The operating frequency and inductor selection are in- terrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. Why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge and switching losses. Also, at higher frequency the duty cycle of body diode conduction is higher, which results in lower efficiency. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

For a given ripple, the inductance terms in continuous mode are as follows:

$$L_{BOOST} > \frac{V_{IN(MIN)}{}^2 * (V_{OUT} - V_{IN(MIN)}) * 1000}{f * \Delta I_L * V_{OUT}{}^2}\ uH$$

$$L_{BUCK} > \frac{V_{OUT} * (V_{IN(MAX)} - V_{OUT}) * 1000}{f * \Delta I_L * V_{IN(MAX)}}\ uH$$

where: f is operating frequency, kHz

VIN(MIN) is minimum input voltage, V

VIN(MAX) is maximum input voltage, V

VOUT is output voltage, V

ΔIL is maximum inductor ripple current, A, usually select 20~40% maximum current.

The inductor value also has secondary effects. The tran- sition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by RSENSE. Lower inductor values (higher ΔIL) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease. Once the value of L is known, an inductor with low DCR and low core losses should be selected.

10.5 Power MOSFET Selection

Two external power MOSFETs must be selected for controller in the PL3901 : one N-channel MOSFET for the mainswitch, and one N-channel MOSFET for the synchronous switch.

The peak-to-peak gate drive levels are set by the INTVCC voltage. This voltage is typically 5.4V during start-up (see EXTVCC pin connection). Consequently, logic-level threshold MOSFETs must be used in most applications.Pay close attention to the BVDSS specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance RDS(ON), Miller capacitance CMILLER, input voltage and maximum output current. Miller capacitance, CMILLER, can be approximated from the gate charge curve usually provided on the MOSFET manufacturer's data sheet. CMILLER is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in VDS. This result is then multiplied by the ratio of the application applied VDS to the gate charge curve specified VDS. In boost mode ,When the IC is operating in continuous mode, the duty cycles for the main and synchronous MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}}$$

If the maximum output current is IOUT(MAX) and each channel takes one half of the total output current, the MOSFET power dissipations in each channel at maximum output current are given by:

$$P_{MAIN} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^2} \bullet \left(\frac{I_{OUT(MAX)}}{2}\right)^2 \bullet (1+\delta) \bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{OUT(MAX)}}{2 \bullet V_{IN}} \bullet C_{MILLER} \bullet f$$

$$P_{SYNC} = \frac{V_{IN}}{V_{OUT}} \bullet \left(\frac{I_{OUT(MAX)}}{2}\right)^2 \bullet (1+\delta) \bullet R_{DS(ON)}$$

where d is the temperature dependency of RDS(ON) (ap- proximately 1Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

Both MOSFETs have I2R losses while the bottom N-channel equation includes an additional term for transition losses, which are highest at low input voltages. For high VIN the high current efficiency generally improves with larger MOSFETs, while for low VIN the transition losses rapidly increase to the point that the use of a higher RDS(ON) device with lower CMILLER actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the bottom switch duty factor is low or during overvoltage when the synchronous switch is on close to 100% of the period.

The term (1+ d) is generally given for a MOSFET in the form of a normalized RDS(ON) vs Temperature curve, but d = 0.005/°C can be used as an approximation for low voltage MOSFETs.

10.6 CIN and COUT Selection

In the boost region, input current is continuous. In the buck region, input current is discontinuous. In the buck region, the selection of input capacitor CIN is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

$$I_{CIN} = I_{OUT(MAX)} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

This input current has a maximum at VIN = 2VOUT, ICIN(MAX) = IOUT(MAX)/2.

In the boost region, COUT must be capable of reducing the output voltage ripple because of the discontinuous output current. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{(BOOST,Cap)} = \frac{I_{OUT(MAX)} * (V_{OUT} - V_{IN(MIN)})}{C_{OUT} * V_{OUT} * f} V$$

where COUT is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{(BOOST,ESR)} = I_{OUT(MAX,BOOST)} * ESR$$

In buck mode, VOUT ripple is given by:

$$\Delta V_{OUT} \leq \Delta I_L * \left(ESR + \frac{1}{8 * f * C_{OUT}} \right)$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

10.7 2-Phase Operation

For output loads that demand high current, two PL3901 s can be cascaded to run out-of-phase to provide more output current and at the same time to reduce input and output voltage ripple. The PLLIN/MODE pin allows the PL3901 to synchronize to the CLKOUT signal of another PL3901 . The CLKOUT signal can be connected to the PLLIN/MODE pin of the following PL3901 stage to line up both the frequency and the phase of the entire system.

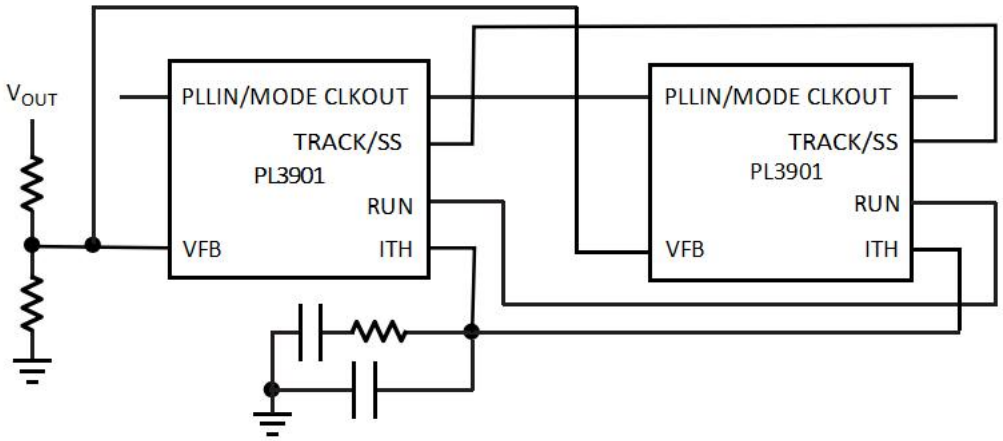


Fig 10.7 2-Phase Operation

10.8 Setting Output Voltage

The PL3901 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 10.8. The regulated output voltage is determined by:

$$V_{OUT} = 1.2V \left(1 + \frac{R_B}{R_A} \right)$$

Great care should be taken to route the VFB line away from noise sources, such as the inductor or the SW line. Also keep the VFB node as small as possible to avoid noise pickup.

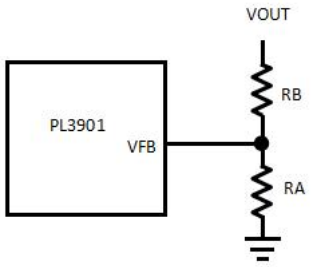


Fig 10.8 Setting Output Voltage

10.9 Soft-Start (TRACK/SS Pin)

The start-up of VOUT is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the internal 1.2V reference, the PL3901 regulates the VFB pin voltage to the voltage on the TRACK/SS pin instead of 1.2V.

Soft-start is enabled by simply connecting a capacitor from the TRACK/SS pin to ground, as shown in Fig10.9An internal 10 μ A current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The PL3901 will regulate the VFB pin (and hence, VOUT) according to the voltage on the TRACK/SS pin, allowing VOUT to rise smoothly from VIN to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{1.2V}{10\mu A}$$

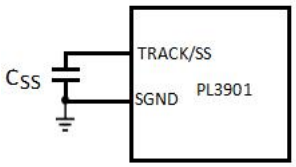


Fig10.9 Using the TRACK/SS Pin to Program Soft-Start

10.10 INTVCC Regulators

The PL3901 features internal P-channel low dropout linear regulators (LDO) that supply power at the INTVCC pin from either the VBIAS supply pin or the EXTVCC pin depending on the connection of the EXTVCC pin. INTVCC powers the gate drivers and much of the PL3901's internal circuitry. The VBIAS LDO and the EXTVCC LDO regulate INTVCC to 5.4V. Each of these can supply at least 50mA and must be bypassed to ground with a minimum of 4.7 μ F ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the max- imum junction temperature rating for the PL3901 to be exceeded. The INTVCC current, which is dominated by the gate charge current, may be supplied by either the VBIAS LDO or the EXTVCC LDO. When the voltage on the EXTVCC pin is less than 4.8V, the VBIAS LDO is enabled. In this case, power dissipation for the IC is highest and is equal to VBIAS • IINTVCC. The gate charge current is dependent on operating frequency, as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics. For example, at 70° C ambient temperature, the PL3901 INTVCC current is limited to less than 27mA in the QFN package from a 56V VBIAS supply when not using the EXTVCC supply:

TJ = 70° C + (27mA)(56V)(53° C/W) = 150° C

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (PLLIN/MODE= INTVCC) at maximum VIN.

When the voltage applied to EXTVCC rises above 4.8V, the VIN LDO is turned off and the EXTVCC LDO is enabled. The EXTVCC LDO remains on as long as the voltage applied to EXTVCC remains above 4.55V. The EXTVCC LDO attempts to regulate the INTVCC voltage to 5.4V, so while EXTVCC is less than 5.4V, the LDO is in dropout and the INTVCC voltage is approximately equal to EXTVCC. When EXTVCC is greater than 5.4V, up to an absolute maximum of 30V, INTVCC is regulated to 5.4V.

Significant thermal gains can be realized by powering INTVCC from an external supply. Tying the EXTVCC pin to a 5V supply reduces the junction temperature in the previous example from 150° C to 77° C in a QFN package:

TJ = 70° C + (27mA)(5V)(53° C/W) = 77° C

If more current is required through the EXTVCC LDO than is specified, an external Schottky diode can be added be-tween the EXTVCC and INTVCC pins. Make sure that in all cases EXTVCC ≤ VBIAS (even at start-up and shutdown).

The following list summarizes possible connections for EXTVCC:

EXTVCC Grounded. This will cause INTVCC to be powered from the internal 5.4V regulator resulting in an efficiency penalty at high input voltages.

EXTVCC Connected to an External Supply. If an external supply is available in the 5V to 30V range, it may be used to provide power. Ensure that EXTVCC is always lower than VBIAS.

Topside MOSFET Driver Supply (CB, DB)

External bootstrap capacitors CB connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor CB in the Block Diagram is charged though external diode DB from INTVCC when the SW pin is low. When one of the topside MOSFETs is to be turned on, the driver places the CB voltage across the gate and source of the desired MOSFET. This enhances the MOS- FET and turns on the topside switch. The switch node voltage, SW, rises to VOUT and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the output voltage: VBOOST = VOUT + VINTVCC. The value of the boost capacitor CB needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than VOUT(MAX).

The external diode DB can be a Schottky diode or silicon diode, but in either case it should have low leakage and fast recovery. Pay close attention to the reverse leakage at high temperatures where it generally increases substantially.

Each of the topside MOSFET drivers includes an internal charge pump that delivers current to the bootstrap capacitor from the BOOST pin. This charge current maintains the bias voltage required to keep the top MOSFET on continuously during dropout/overvoltage conditions. The Schottky/sil- icon diodes selected for the topside drivers should have a reverse leakage less than the available output current the charge pump can supply.

A leaky diode DB in the boost converter can not only prevent the top MOSFET from fully turning on but it can also completely discharge the bootstrap capacitor CB and create a current path from the input voltage to the BOOST pin to INTVCC. This can cause INTVCC to rise if the diode leakage exceeds the current consumption on INTVCC. This is particularly a concern in Burst Mode operation where the load on INTVCC can be very small. The external Schottky or silicon diode should be carefully chosen such that INTVCC never gets charged up much higher than its normal regulation voltage.

10.11 Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating on-chip (such as an INTVCC short to ground), the overtemperature shutdown circuitry will shut down the PL3901. When the junction temperature exceeds approximately 150° C, the overtemperature circuitry disables the INTVCC LDO, causing the INTVCC supply to collapse and effectively shut down the entire PL3901 chip. Once the junction temperature drops back to approximately 135° C, the INTVCC LDO turns back on. Long term overstress (TJ > 150° C) should be avoided as it can degrade the performance or shorten the life of the part.

Since the shutdown may occur at full load, beware that the load current will result in high power dissipation in the body diodes of the top MOSFETs. In this case, PGOOD output may be used to turn the system load off.

10.12 Phase-Locked Loop and Frequency Synchronization

The PL3901 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter and a voltage-controlled oscillator (VCO). The phase detector is an edge-sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

If the external clock frequency is greater than the internal oscillator’ s frequency, fOSC, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than fOSC,current is sunk continuously, pulling down the VCO input. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, CLP , holds the voltage at the VCO input.

Typically, the external clock (on the PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 0.4V.

Note that the PL3901 can only be synchronized to an external clock whose frequency is within range of the PL3901’s internal VCO, which is nominally 55kHz to 1MHz. This is guaranteed to be between 75kHz and 850kHz.

Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchro- nization frequency. The VCO’ s input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free-running frequency be near external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

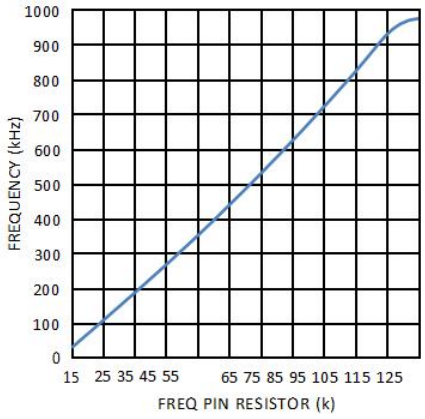


Figure 10.11 Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

Table 2 summarizes the different states in which the FREQ pin can be used.

Table 2.

FREQ PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	350kHz
INTVCC	DC Voltage	535kHz
Resistor	DC Voltage	50kHz to 900kHz
Any of the Above	External Clock	Phase Locked to External Clock

10.13 Minimum On-Time Considerations

Minimum on-time, tON(MIN), is the smallest time duration that the PL3901 is capable of turning on the bottom MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET.

In forced continuous mode, if the input voltage is close to the output voltage , the controller will begin to skip cycles but the output will continue to be regulated. The minimum on-time for the PL3901 is approximately 110ns.

10.14 Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the greatest improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, five main sources usually account for most of the losses in PL3901 circuits: 1) IC VBIAS current, 2) INTVCC regulator current, 3) I2R losses, 4) bottom MOS- FET transition losses, 5) body diode conduction losses.

1.The VBIAS current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. VBIAS current typically results in a small (<0.1%) loss.

2.INTVCC current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from INTVCC to ground. The resulting dQ/dt is a current out of INTVCC that is typically much larger than the control circuit current. In continuous mode, IGATECHG= f(QT + QB), where QT and QB are the gate charges of the topside and bottom side MOSFETs.

3.DC I2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.

4.Transition losses apply only to the bottom MOSFET(s), and become significant only when operating at low input voltages. Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)\frac{V_{OUT}^3}{V_{IN}} \bullet \frac{I_{OUT(MAX)}}{2} \bullet C_{RSS} \bullet f$$

5.Body diode conduction losses are more significant at higher switching frequency. During the dead time, the loss in the top MOSFETs is IOUT • VDS, where VDS is around 0.7V. At higher switching frequency, the dead time be- comes a good percentage of switching cycle and causes the efficiency to drop.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional efficiency degradation in portable systems. It is very important to include these system-level losses during the design phase.

10.15 Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, VOUT shifts by an amount equal to ΔILOAD(ESR), where ESR is the effective series resistance of COUT. ΔILOAD also begins to charge or discharge COUT generating the feedback error signal that forces the regulator to adapt to the current change and return VOUT to its steady-state value. During this recov- ery time VOUT can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/ or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the Figure 10 circuit will provide an adequate starting point for most applications.

The ITH series RC-CC filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is complete and the particular output capacitor type and value have been determined. The output capacitors must be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1μs to 10μs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET and load resistor directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing RC and the bandwidth of the loop will be increased by de- creasing CC. If RC is increased by the same factor that CC is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1 μ F) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with COUT , causing a rapid drop in VOUT . No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of CLOAD to COUT is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • CLOAD. Thus, a 10 μ F capacitor would require a 250 μ s rise time, limiting the charging current to about 200mA.

10.16 Design Example

As a design example, assume VIN = 12V (nominal), VIN = 22V (max), VOUT = 24V, IOUT(MAX) = 8A, VSENSE(-MAX) = 60mV, and f = 350kHz.

The components are designed based on single channel operation. The inductance value is chosen first based on a 30% ripple current assumption. Tie the PLLIN/MODE pin to GND, generating 350kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{IN}}{f \bullet L}\left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

The largest ripple happens when VIN = 1/2VOUT = 12V, where the average maximum inductor current for each channel is:

$$I_{MAX} = \left(\frac{I_{OUT(MAX)}}{2}\right) \bullet \left(\frac{V_{OUT}}{V_{IN}}\right) = 8A$$

A 6.8μH inductor will produce a 31% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 9.25A.

$$R_{SENSE} \leq \frac{60mV}{9.25A} = 0.006\Omega$$

The RSENSE resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances:

Choosing 1% resistors: RA = 5k and RB = 95.3k yields an output voltage of 24.072V.

The power dissipation on the top side MOSFET in each chan- nel can be easily estimated. Choosing a Vishay Si7848BDP MOSFET results in: RDS(ON) = 0.012Ω, CMILLER = 150pF.At maximum input voltage with T (estimated) = 50°C:

$$P_{MAIN} = \frac{(24V - 12V)\,24V}{(12V)^2} \bullet (4A)^2 \bullet [1 + (0.005)(50°C - 25°C)] \bullet 0.008\Omega + (1.7)(24V)^3 \frac{4A}{12V}(150pF)(350kHz) = 0.7W$$

COUT is chosen to filter the square current in the output. The maximum output current peak is:

$$I_{OUT(PEAK)} = 8 \bullet \left(1 + \frac{31\%}{2}\right) = 9.3A$$

A low ESR (5mΩ) capacitor is suggested. This capacitor will limit output voltage ripple to 46.5mV (assuming ESR dominate ripple).

10.17 PCB Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

Check the following in your layout:

1.Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of CINTVCC must return to the combined COUT (–) ter- minals. The path formed by the top N-channel MOSFET, Schottky diode and the CIN capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.

2.Does the PL3901 VFB pin's resistive divider connect to the (+) terminal of COUT? The resistive divider must be connected between the (+) terminal of COUT and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).

3.Are the SENSE– and SENSE+ leads routed together with minimum PC trace spacing? The filter capacitor between SENSE+ and SENSE – should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.

4.Is the INTVCC decoupling capacitor connected close to the IC, between the INTVCC and the power ground pins? This capacitor carries the MOSFET drivers' cur-rent peaks. An additional 1 μ F ceramic capacitor placed immediately next to the INTVCC and PGND pins can help improve noise performance substantially.

5.Keep the SW, TG, and BOOST nodes away from sensi- tive small-signal nodes. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the PL3901 and occupy minimum PC trace area.

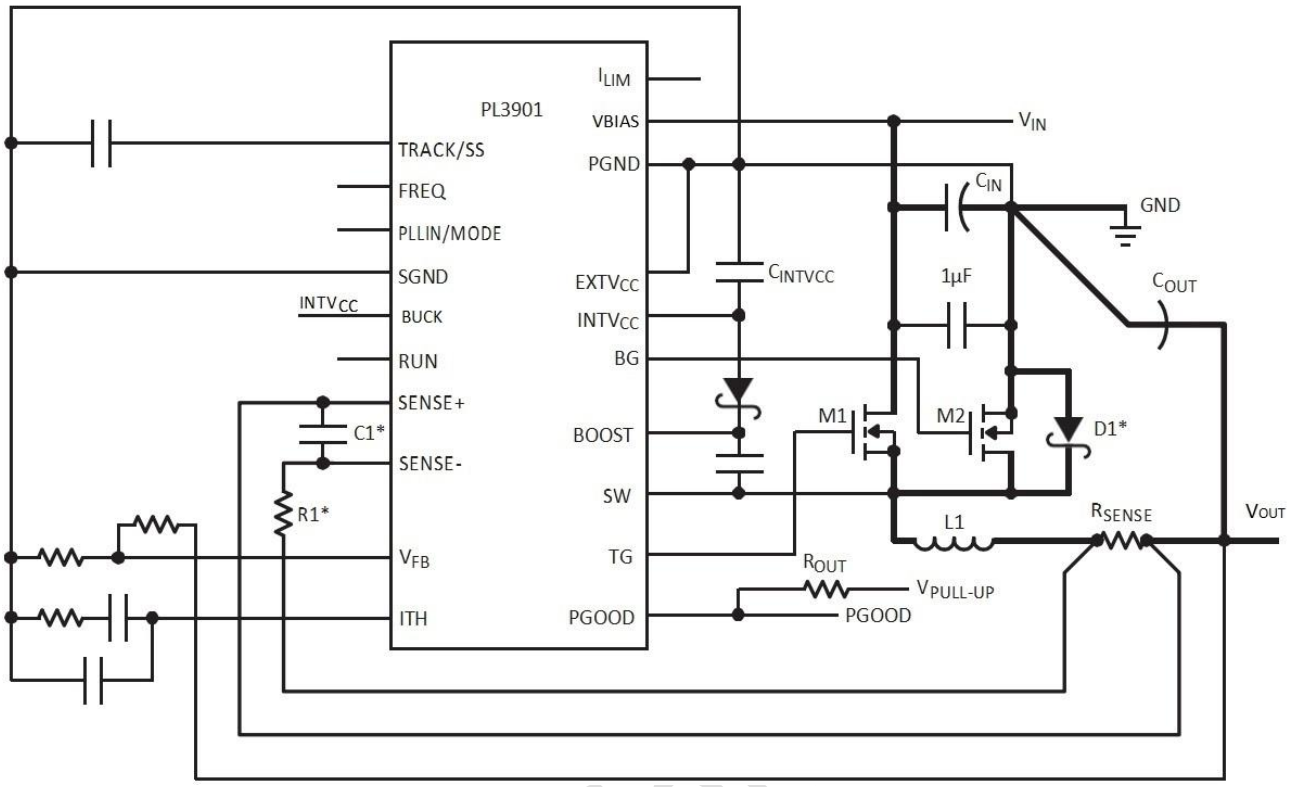


Fig 10.17.1 Recommended Printed Circuit Layout Diagram

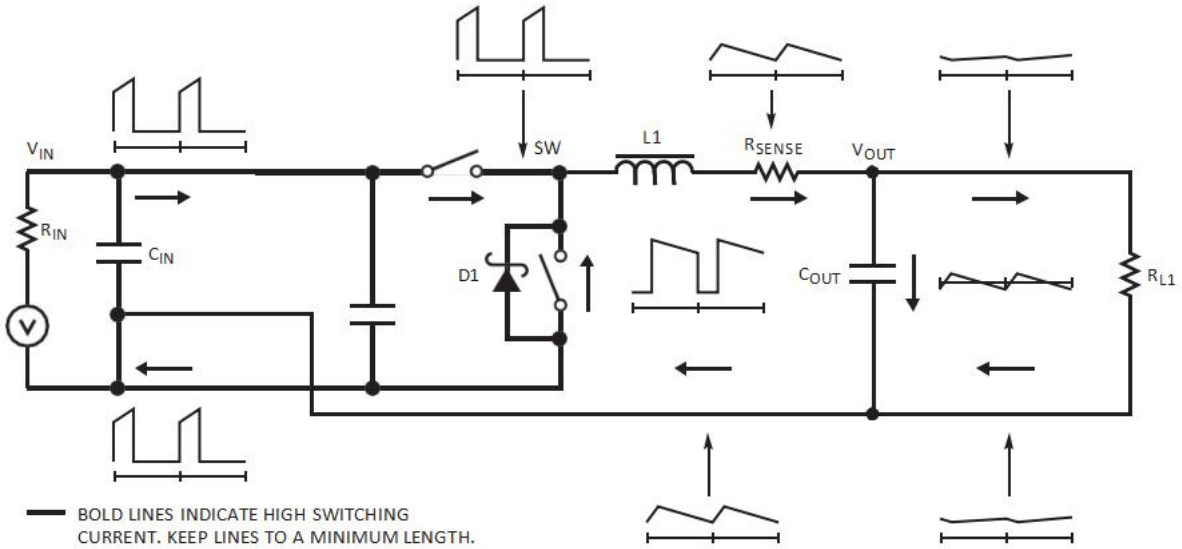


Fig10.17.2 Branch Current Waveforms

10.18 PCB Board Layout Debugging

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be main- tained over the input voltage range down to dropout and until the output load drops below the low current opera- tion threshold—typically 25% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can sug- gest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

Reduce VIN from its nominal level to verify operation of the regulator in dropout. Check the operation of the un-dervoltage lockout circuit by further lowering VIN while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher out- put currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look

for inductive coupling between CIN, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

11 Application Examples

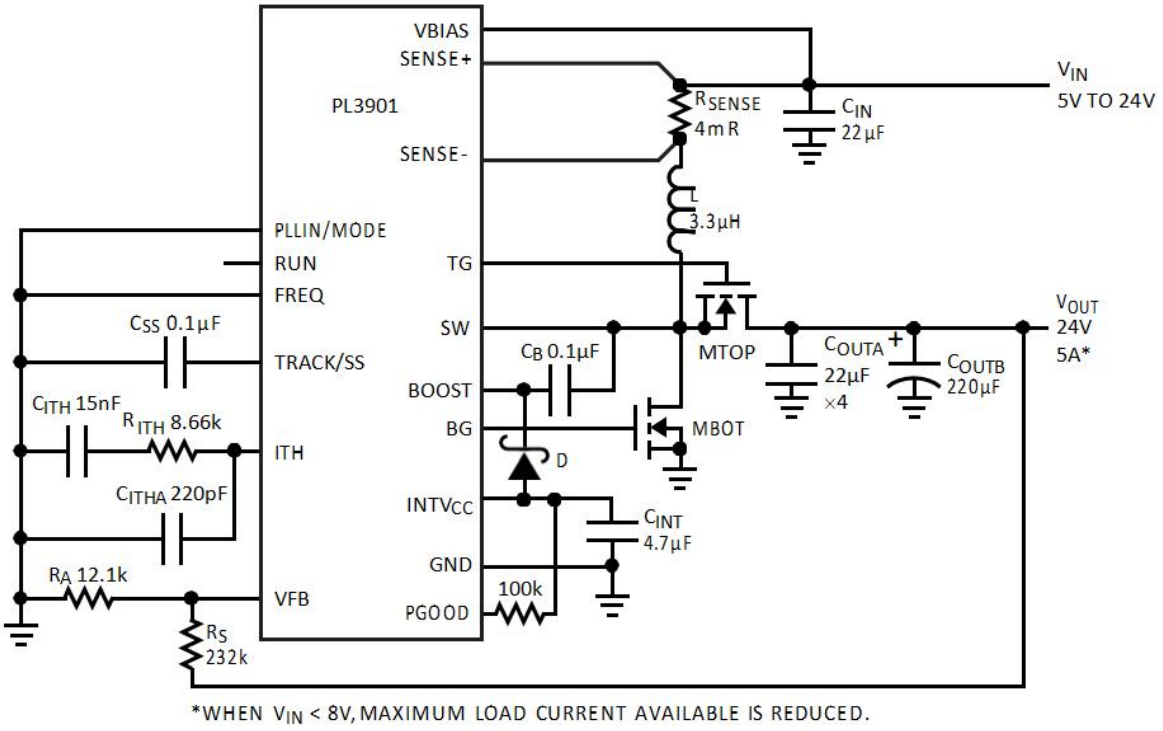


Fig11.1 High Efficiency 24V Boost Converter

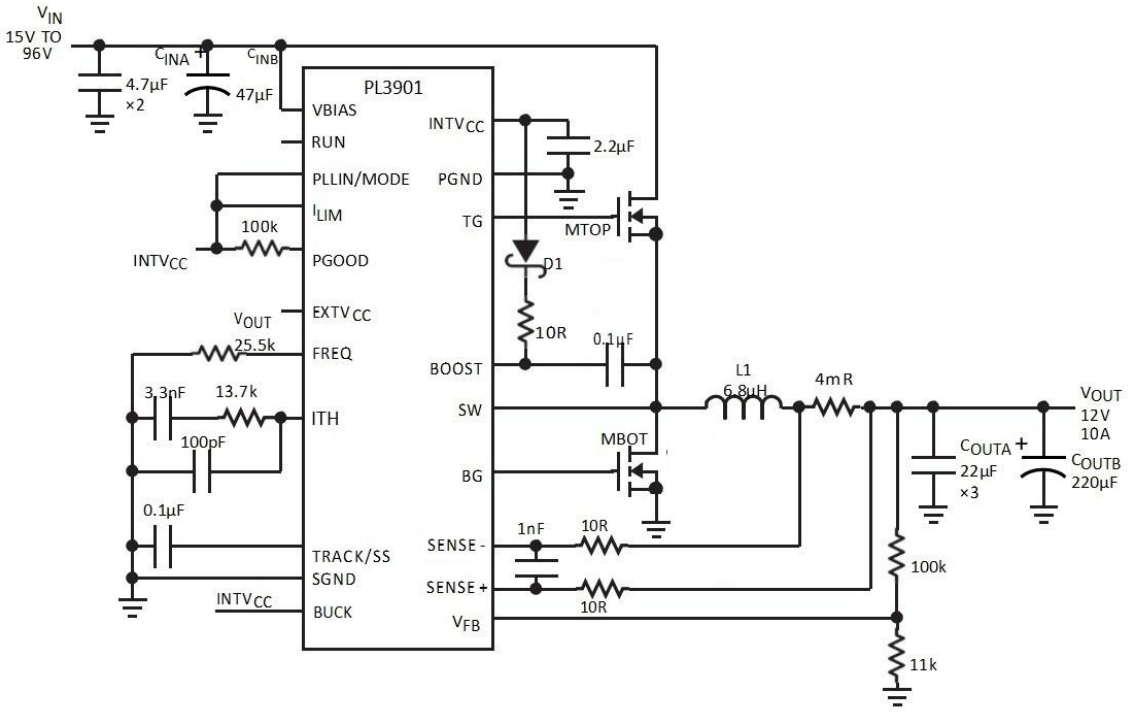


Fig11.2 High Efficiency 12V Buck Converter

11.2 Application Examples

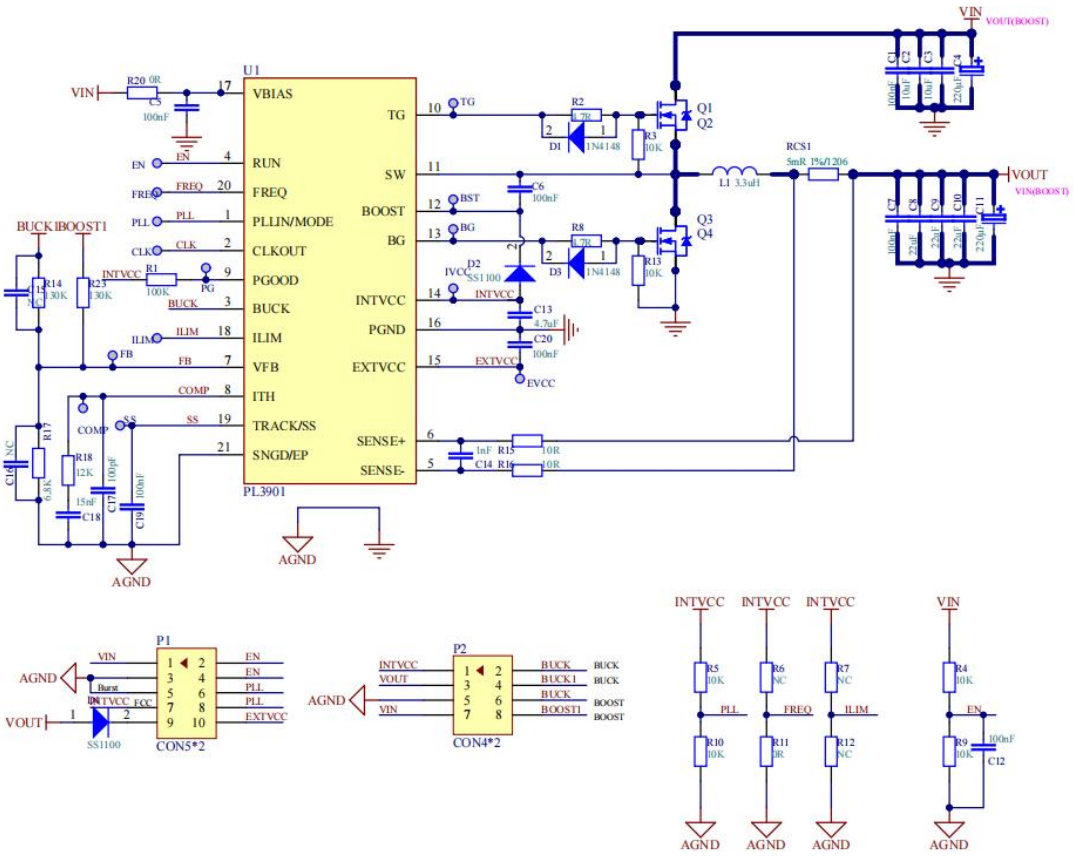


Fig11-2-1 Schematic

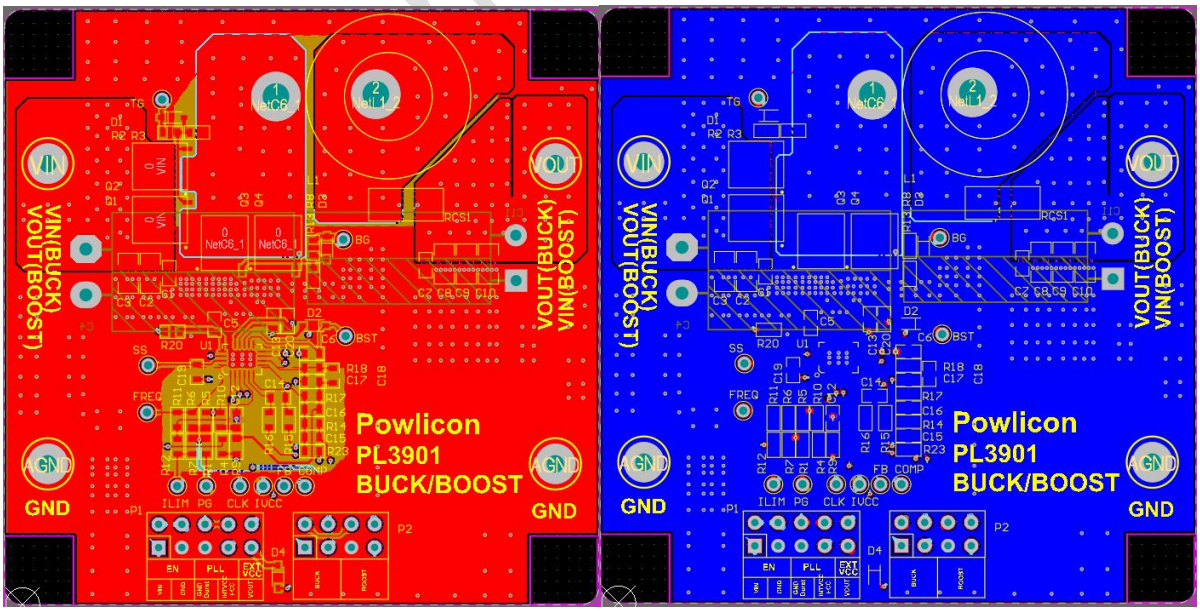
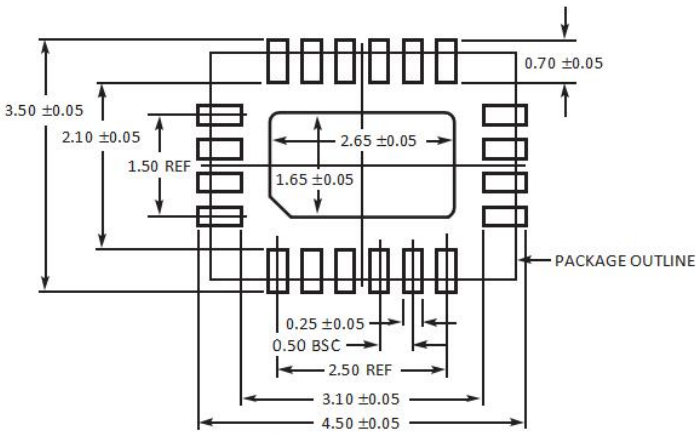


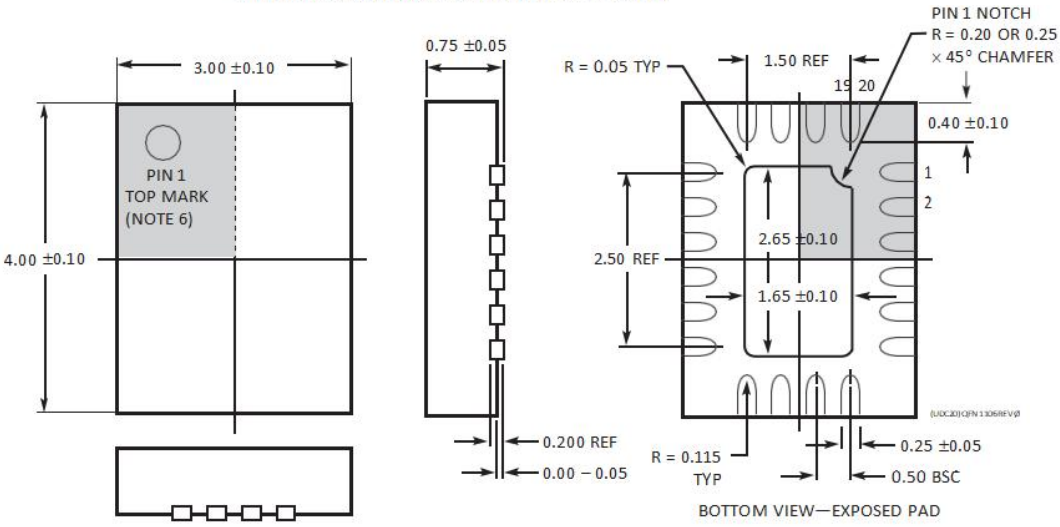
Fig11-2-3 PCB

12 Packaging Information

UDC Package
20-Lead Plastic QFN (3mm × 4mm)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE